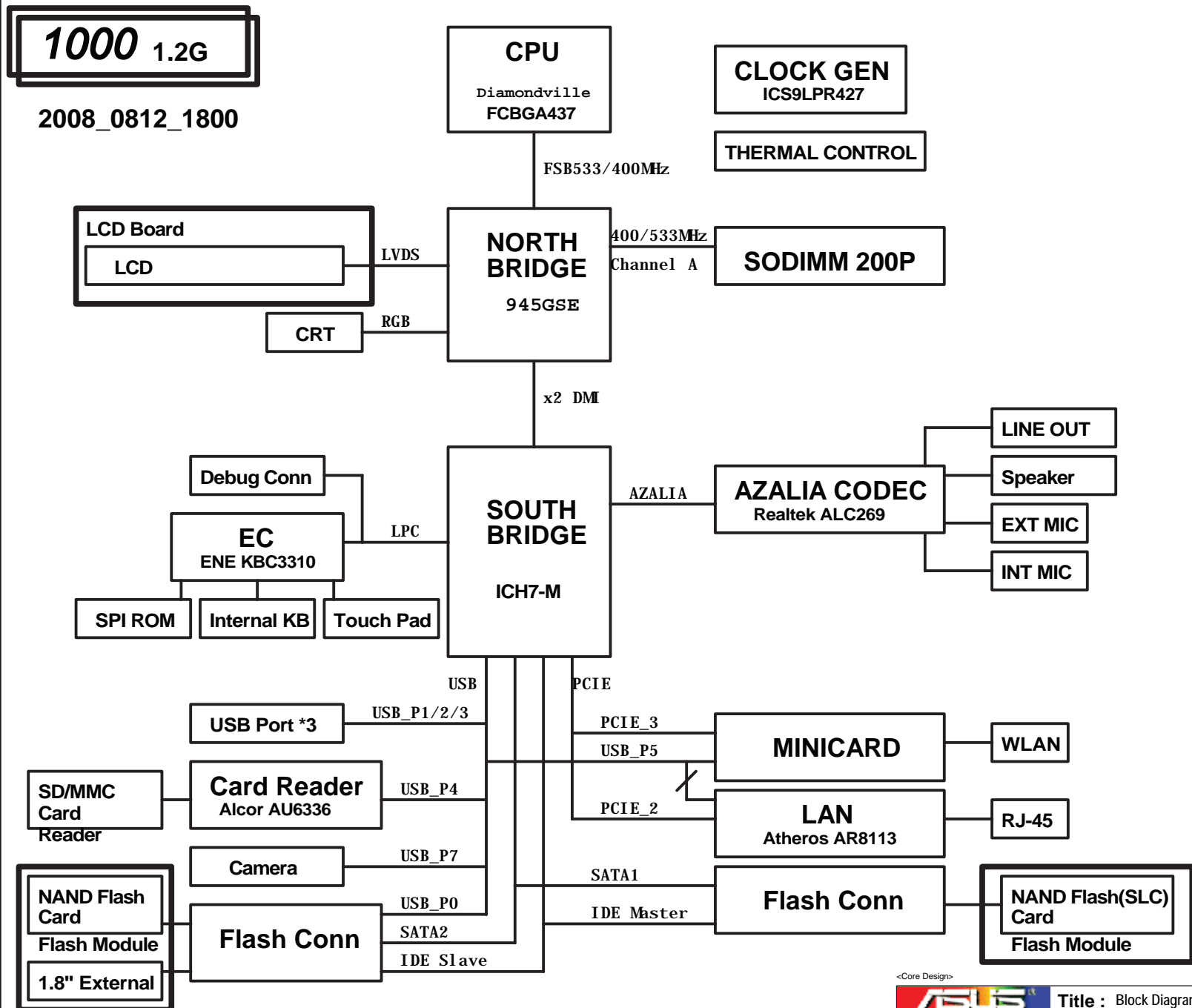


01_Block Diagram
 02_System Setting
 03_Power Sequence
 04_Clock Gen_ICS9LPR426
 05_Diamondville_BUS
 06_Diamondville_PWR
 07_NB-945GMS(HOST)
 08_NB-945GMS(DMI)
 09_NB-945GMS(GRAPHIC)
 10_NB-945GMS(DDR2)
 11_NB-945GMS(PWR)
 12_NB-945GMS(PWR2)
 13_NB-945GMS(GND)
 14_SB-ICH7M(PWR)
 15_SB-ICH7M(1)
 16_SB-ICH7M(2)
 17_SB-ICH7M(3)
 18_DDR2 SODIMM
 19_DDR2 Termination
 20_Onboard VGA
 21_LCD Conn_LID
 22_PCIEx 3.5G & Ext. Antenna
 23_Mini WIFI+ BT
 24_LAN_Atheros AR8113
 25_MDC_RJ11_RJ45
 26_HD + Flash Conn
 27_USB Port
 28_Camera Conn
 29_Card Reader_AU6336C52
 30_Codec_ALC269
 31_Audio_AMP_Jack
 32_EC_ENE KB3310
 33_EC_UART controller
 34_Switch_SPI ROM_Debug Conn
 35_Thermal Sensor_FAN
 36_KB_Touch Pad
 37_LED_THERMTRIP
 38_Discharge
 39_PWR Jack
 40_Srew Hole
 41_EMI
 42_POWER FLOW
 43_Vcore
 44_Power System
 45_Power_+1.8V & VTTDDR
 46_Power_VCCP
 47_Power_+1.5VS & +2.5VS
 48_Power_Charger
 49_EC Pin Define
 49_History



EEE PC 701 PCB version

GPI37	GPI38	GPI39	PCB version
0	0	0	
0	0	0	
0	0	1	
0	0	1	
0	1	0	
0	1	0	
0	1	1	
0	1	1	
1	0	0	
1	0	0	
1	0	1	
1	0	1	
1	1	0	
1	1	0	
1	1	1	
1	1	1	

USB

USB 0	<i>Flash Conn</i>
USB 1	<i>USB Conn</i>
USB 2	<i>USB Conn</i>
USB 3	<i>USB Conn</i>
USB 4	<i>Card Reader</i>
USB 5	<i>Minicard</i>
USB 6	<i>NC</i>
USB 7	<i>Camera</i>


PCIE

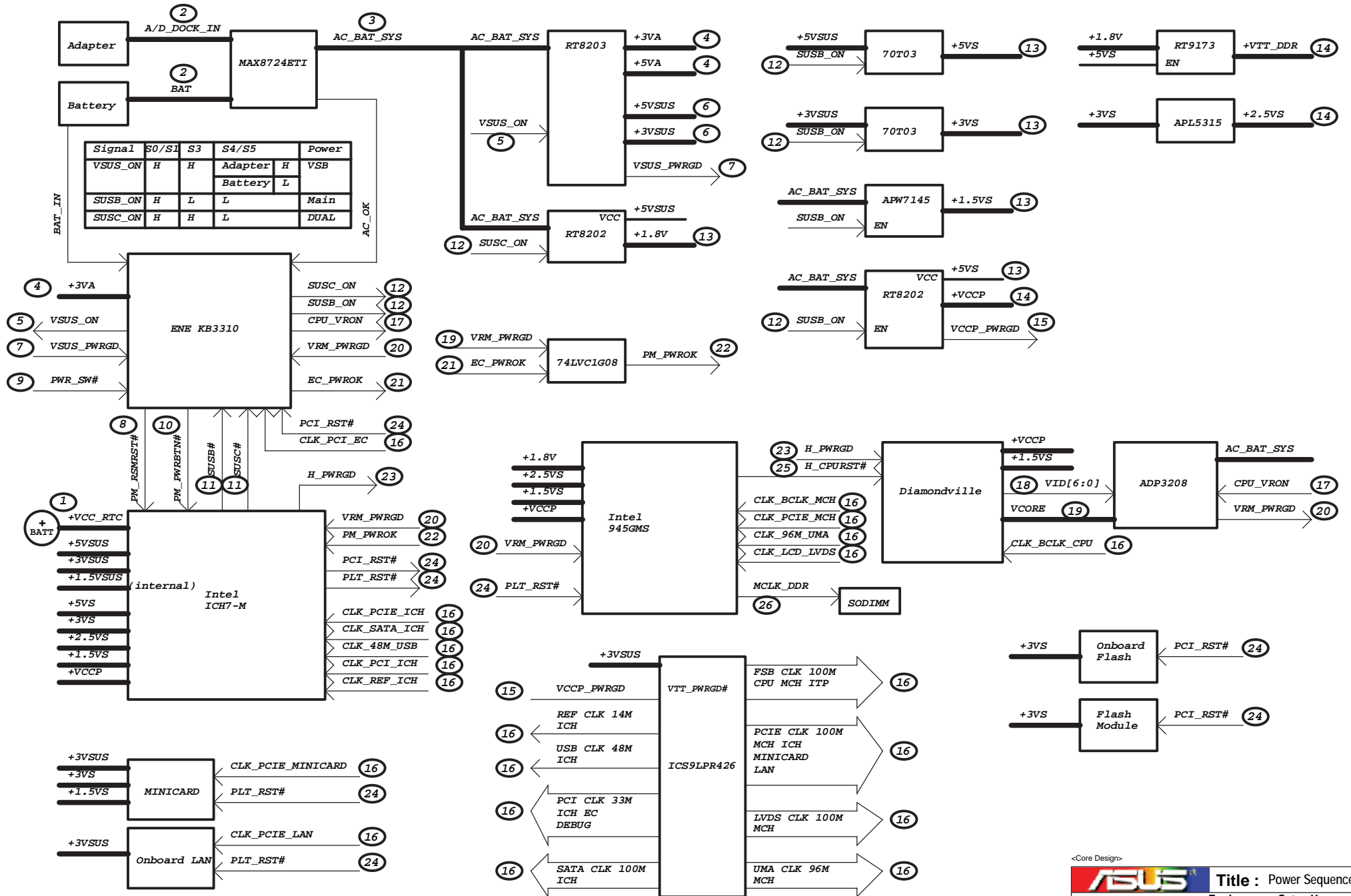
PCIE 1	<i>NC</i>
PCIE 2	<i>LAN</i>
PCIE 3	<i>Minicard</i>
PCIE 4	<i>NC</i>

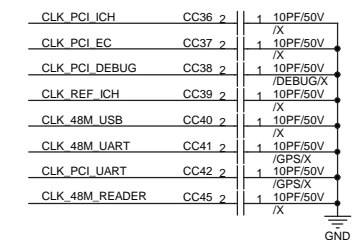
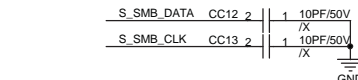
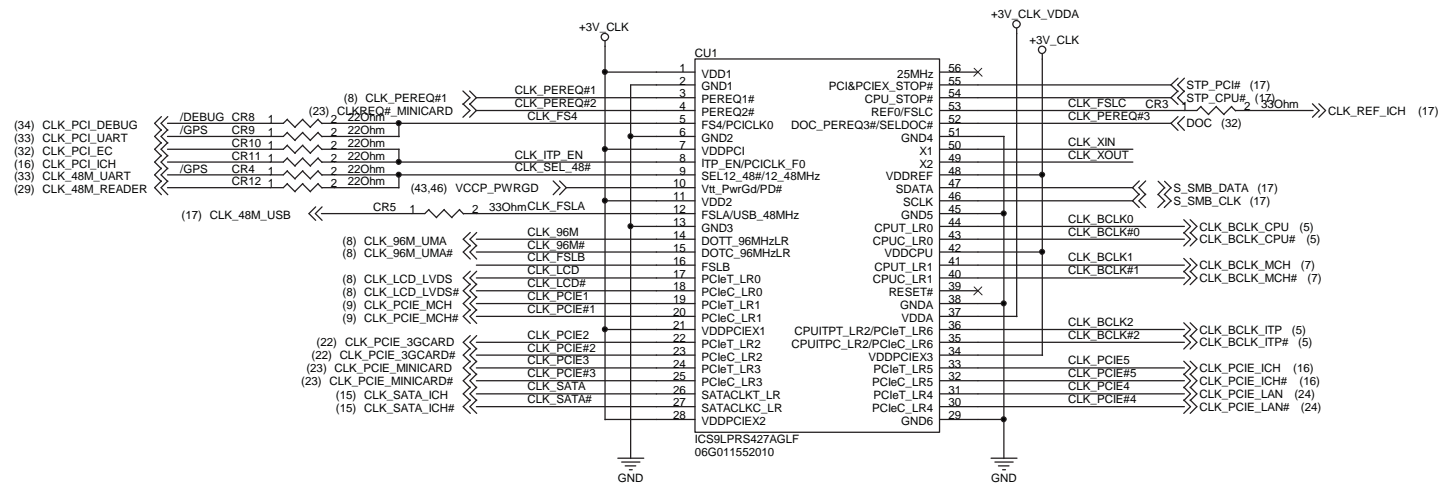
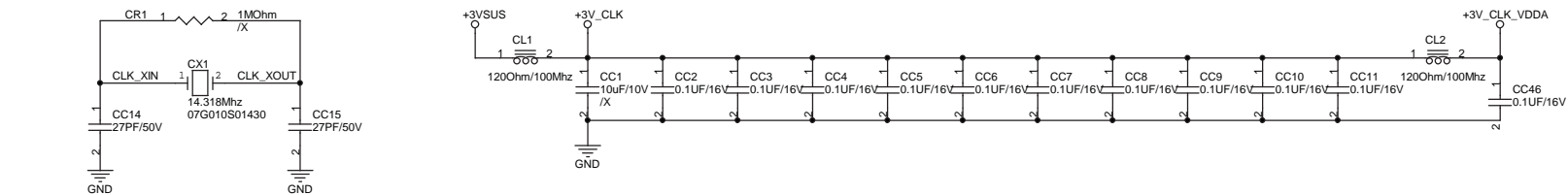
Azalia

ACZ_SDIN0	<i>CODEC</i>
ACZ_SDIN1	<i>MODEM</i>
ACZ_SDIN2	<i>NC</i>

<Core Design>

		Title : System Setting	
ASUSTek Computer INC.		Engineer: Satan_He	
Size A3	Project Name 1000	Rev 1.0G	
Date: Tuesday, August 12, 2008		Sheet 2 of 50	

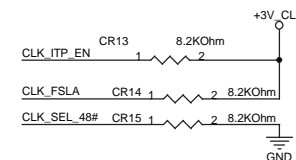
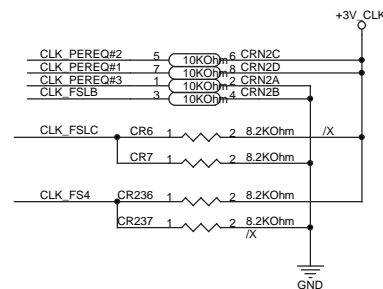




1:Disable
0:Enable

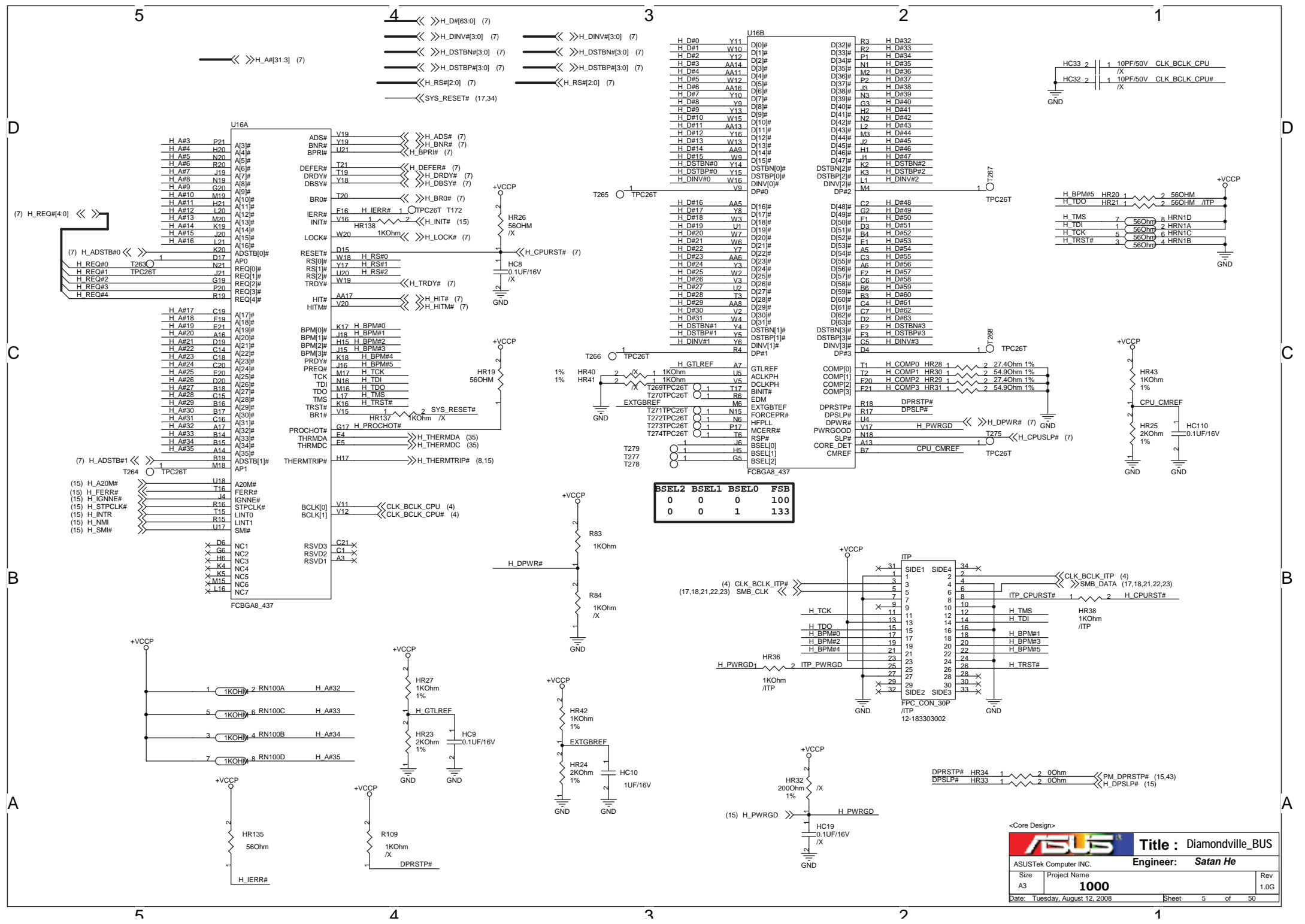
PEREQ1:PCIEx0 & PCIEx1
PEREQ2:PCIEx2 & PCIEx3 & SATA
PEREQ3:PCIEx4 & PCIEx5 & PCIEx6

FSC	FSB	FSA	CPU	PCIE	SATA
0	0	1	133	100	100
1	0	1	100	100	100



<Core Design>

ASUS		Title :Clock Gen_ICS9LPRS427	
ASUSTek Computer INC.		Engineer: Satan He	
Size A3	Project Name 1000	Rev 1.0G	
Date: Tuesday, August 12, 2008		Sheet 4 of 50	

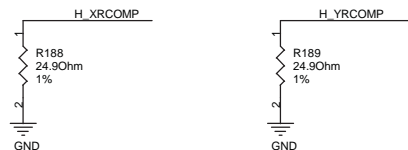




**Power :
+VCCP**

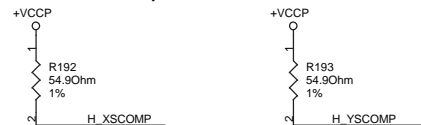
RCOMP

For Calibrating the FSB I/O Buffer



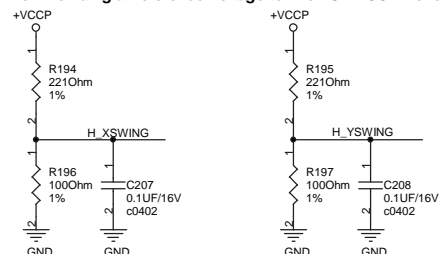
SCOMP

For Slew Rate Compensation on the FSB

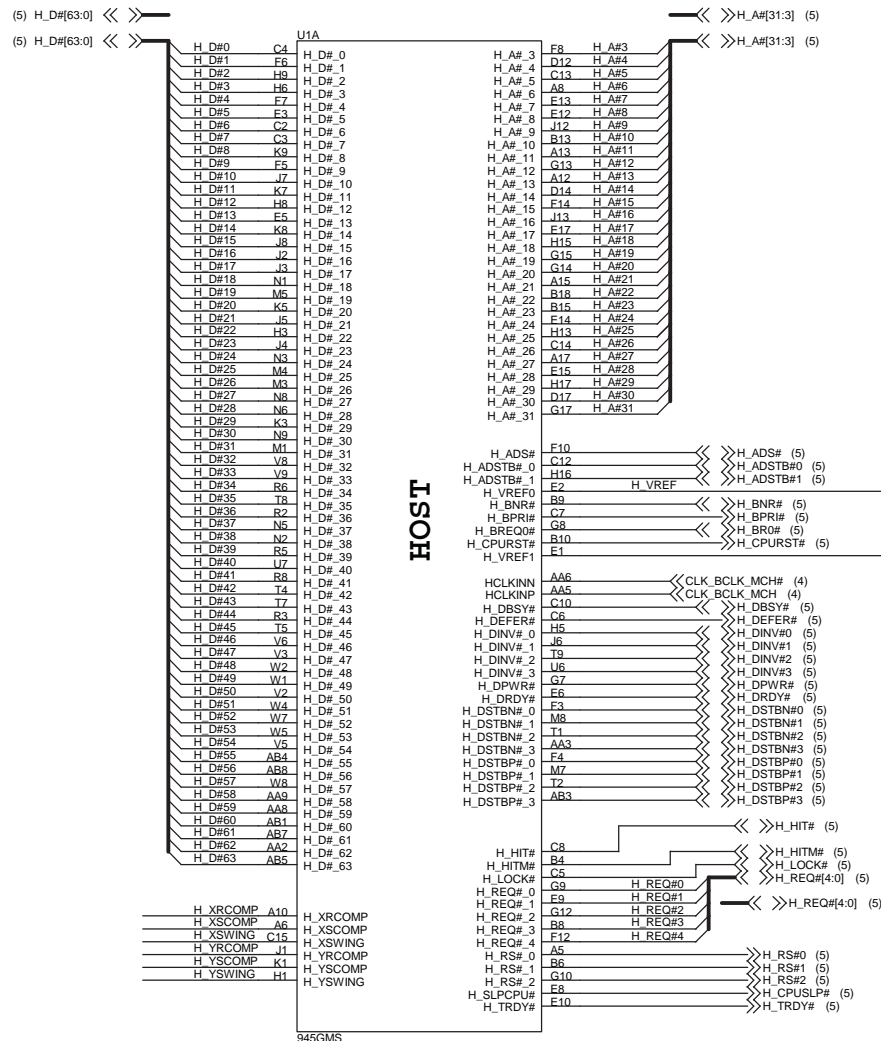


Voltage Swing

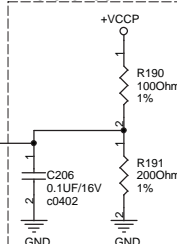
For Providing a Reference Voltage to The FSB RCOMP circuits



Signal voltage level =
0.3125*VCCP
Trace should be 10 mil wide
with 20 mil spacing



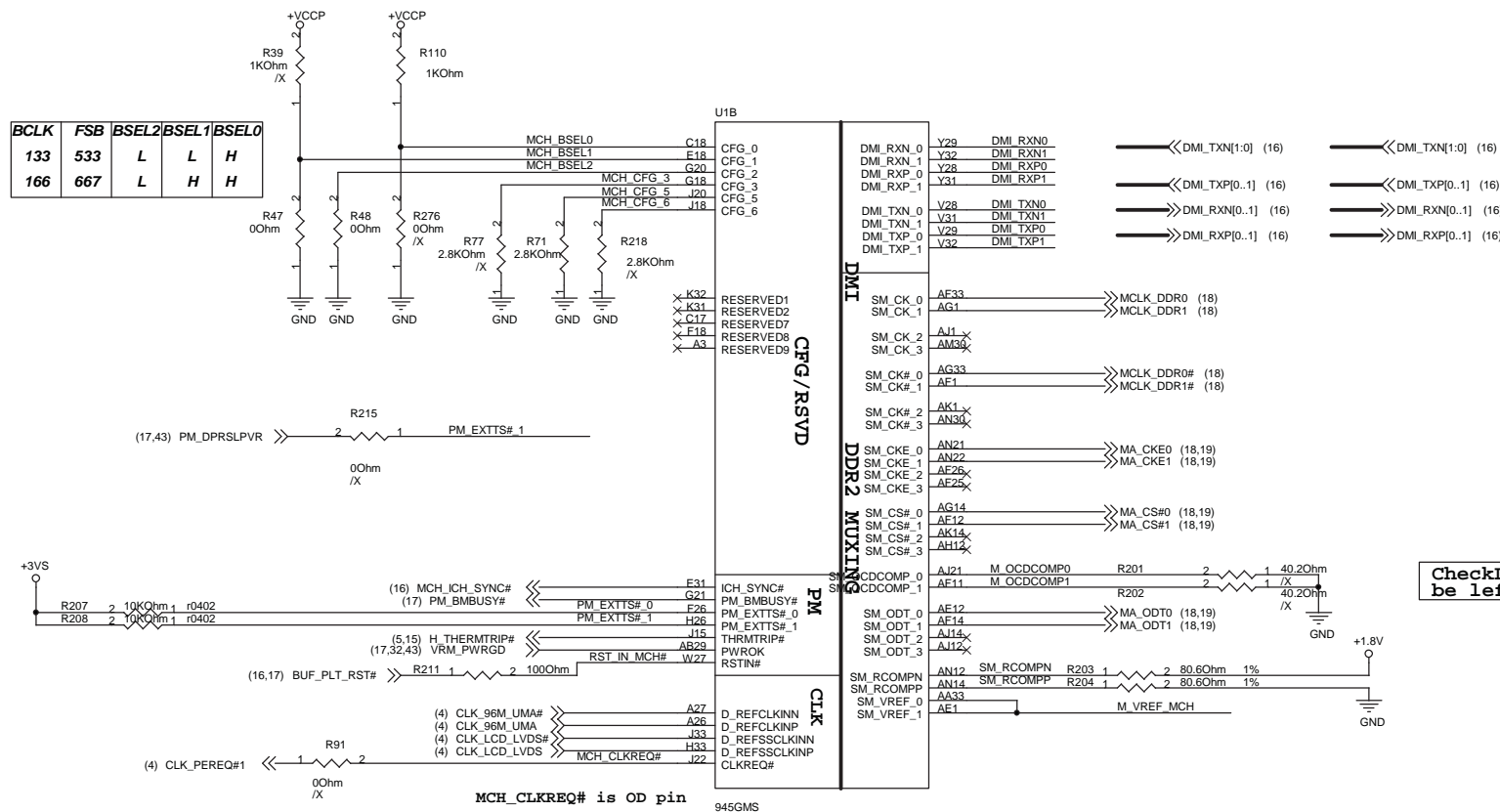
AGTL+ I/O Voltage Reference

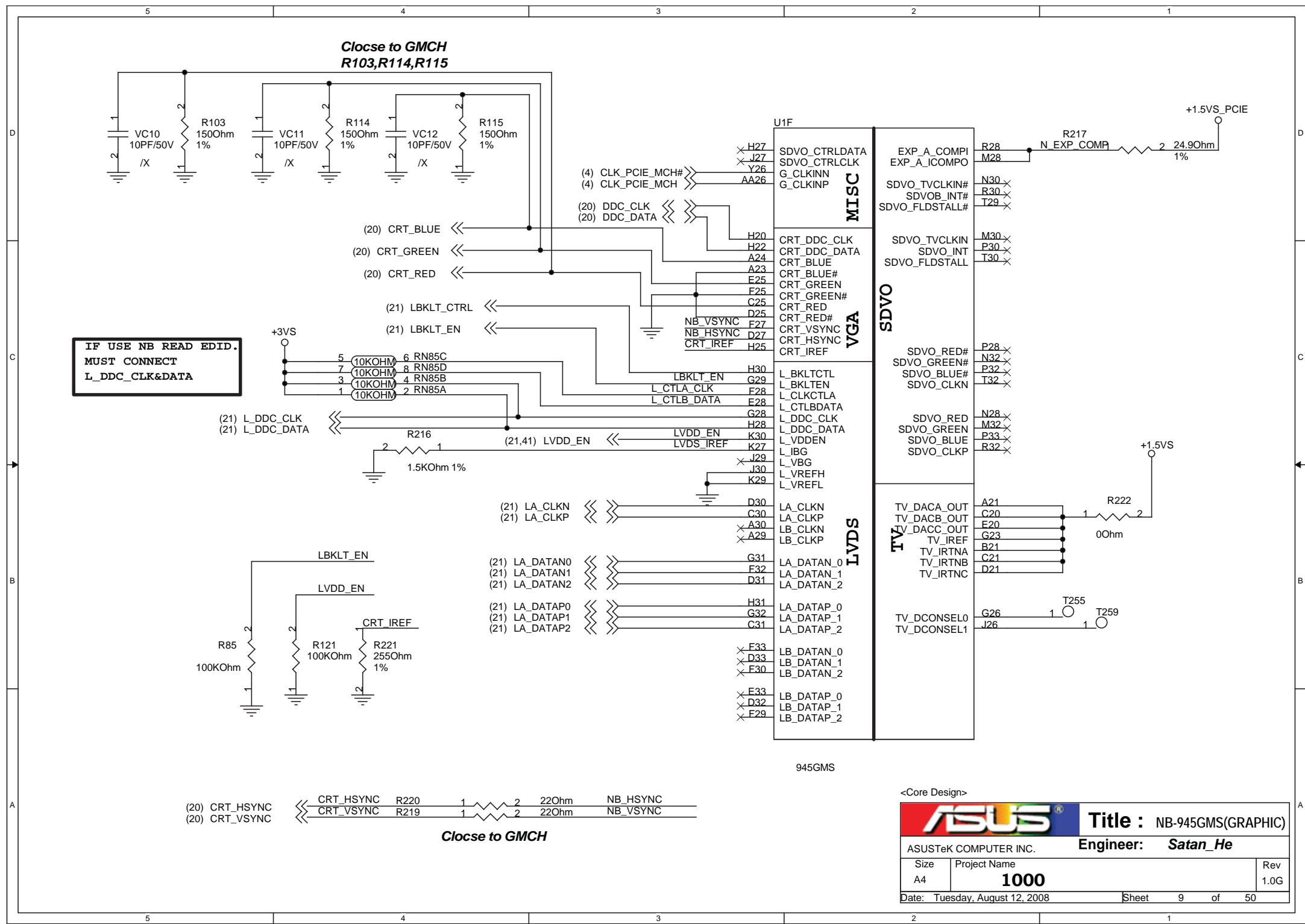


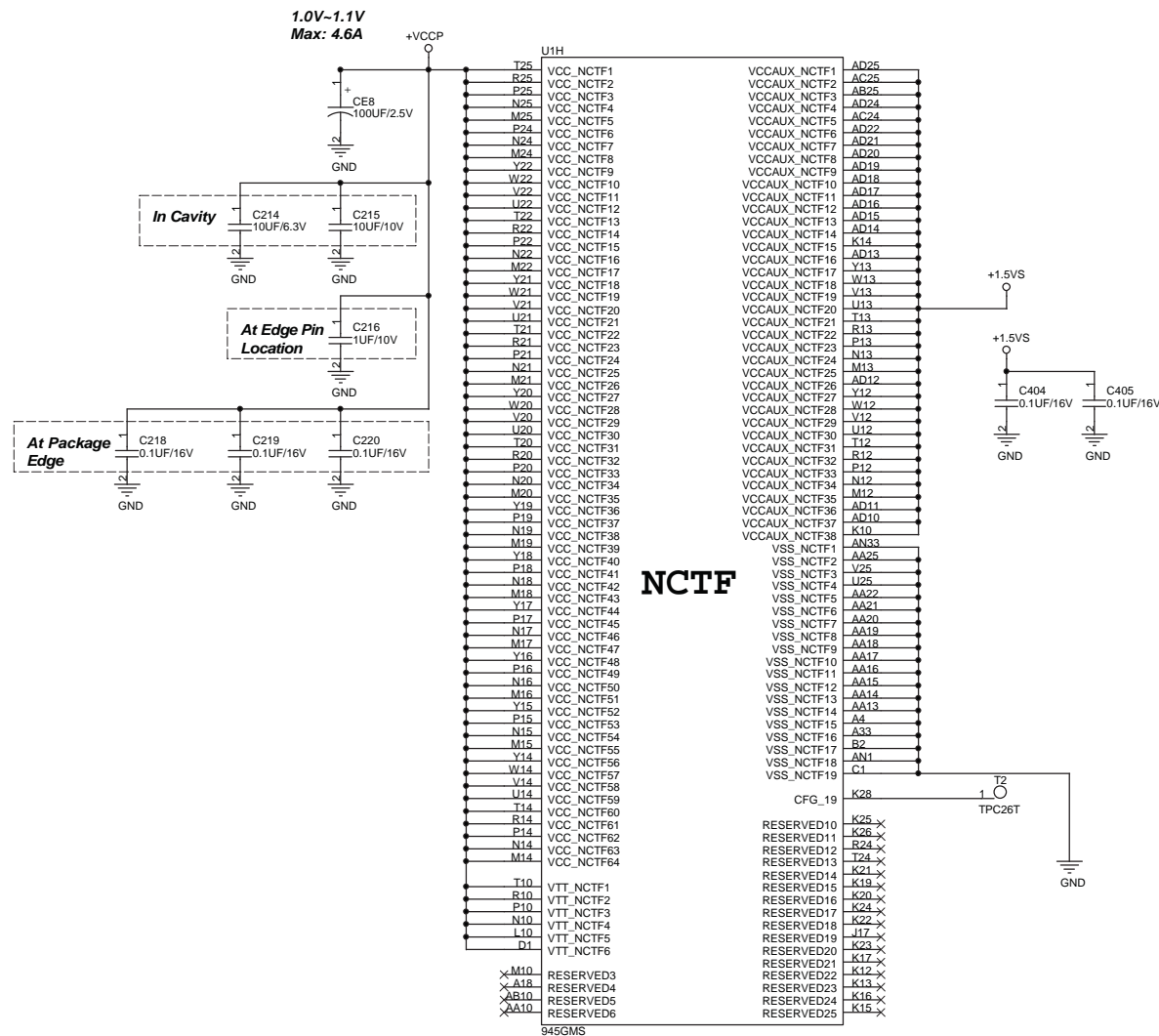
*Layout Note:
0.1uF should be placed 100mils or
less from GMCH pin.*

<Core Design>

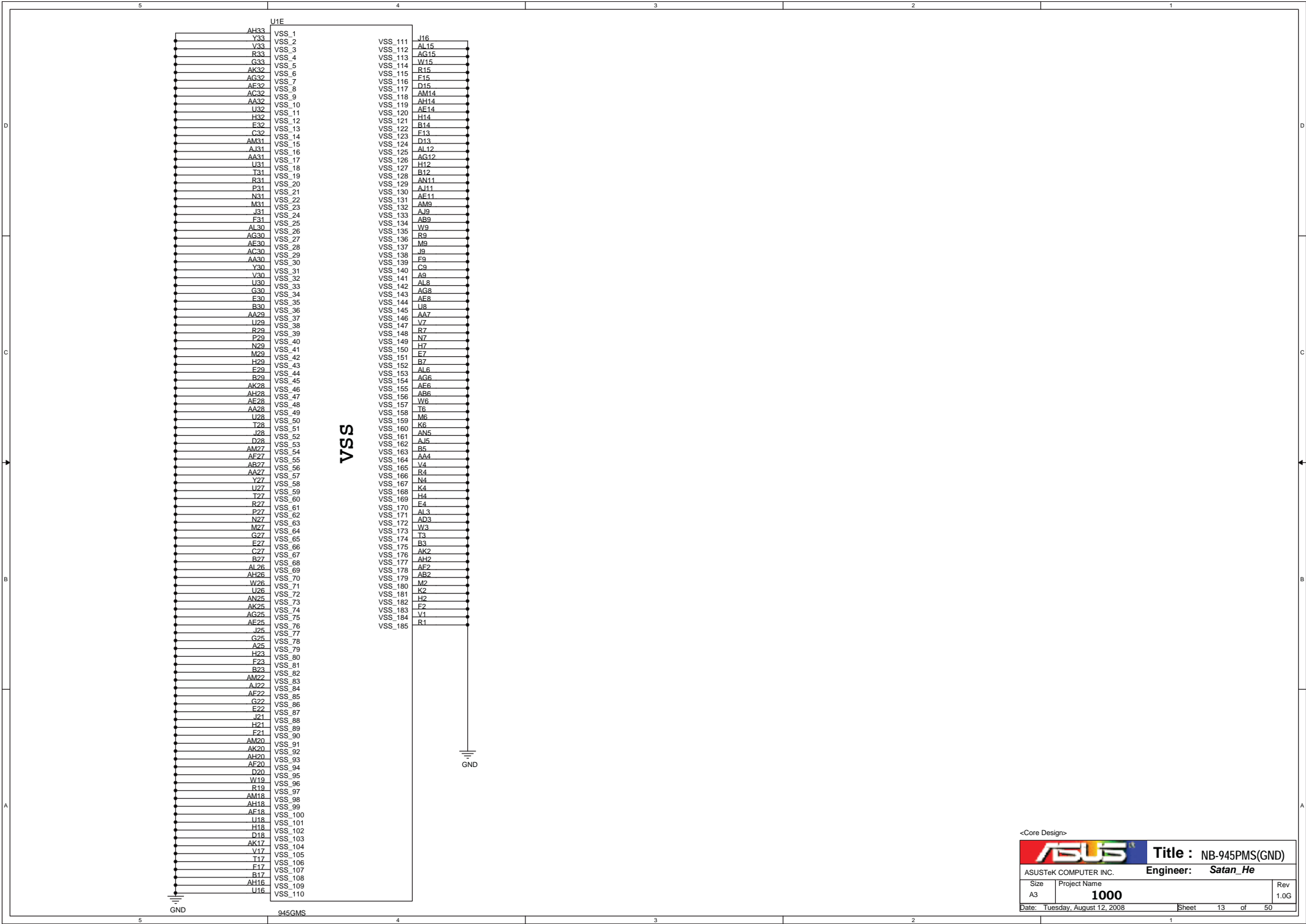
ASUS		Title : NB-945GMS(HOST)	
ASUSTek COMPUTER INC.		Engineer: Satan He	
Size A3	Project Name 1000	Rev 1.0G	
Date: Tuesday, August 12, 2008		Sheet 7 of 50	

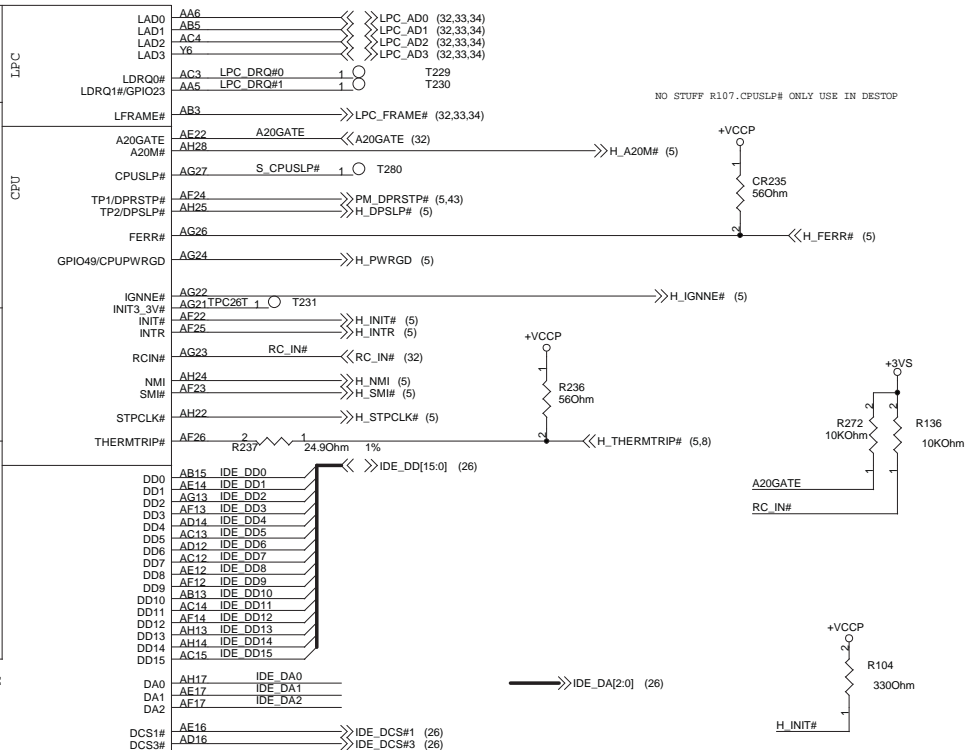
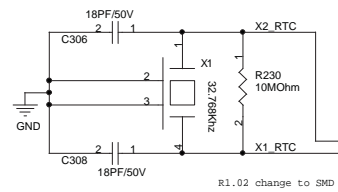


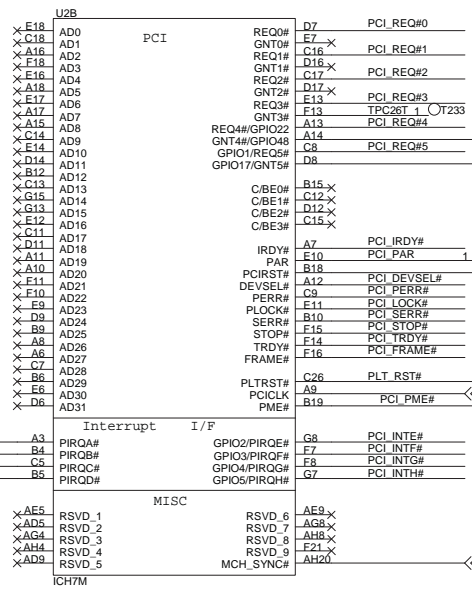




CFG_19(K28) Strapping :
DMI LANE Reversal:
0:Normal Operation (Default)
1.:Reversal Lanes, 3->0,2->1..etc
Note:945GMS doesn't support DMI Lane Reversal

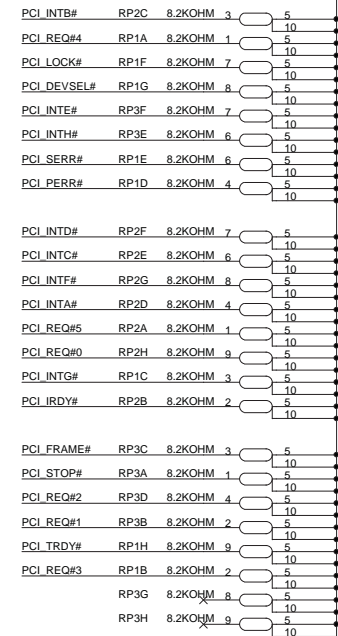






ICH7 Boot BIOS Select		
	GNT#5	GNT#4
LPC	H	H
PCI	H	L
SPI	L	H

Buffer to Reduce Loading on PLT_RST#



When disable port 1, all port will be disabled.

Internal Pull-Up R88

CRB & Checklist

ASUS

Title : SB-ICH7M(2)

ASUSTeK COMPUTER INC.

Engineer: Satan He

Size

Project Name

Custom

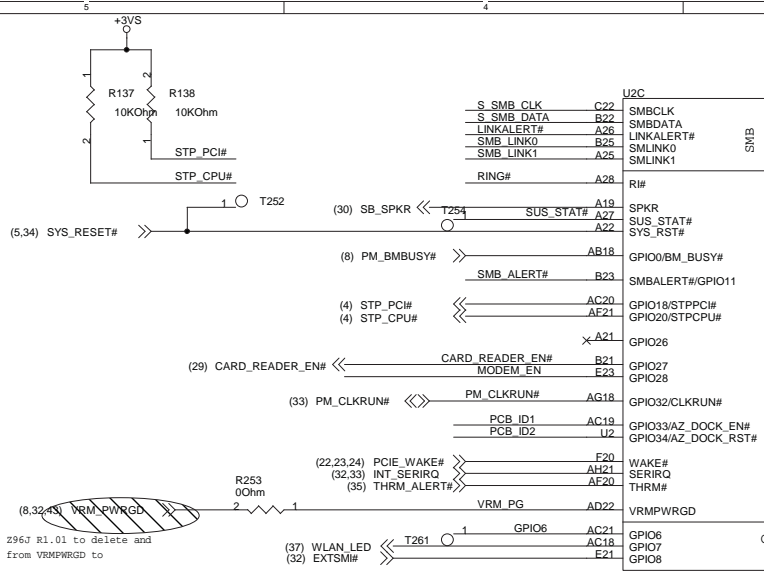
1000

Rev

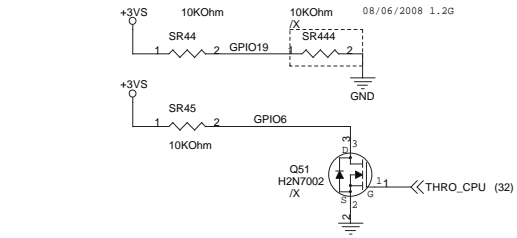
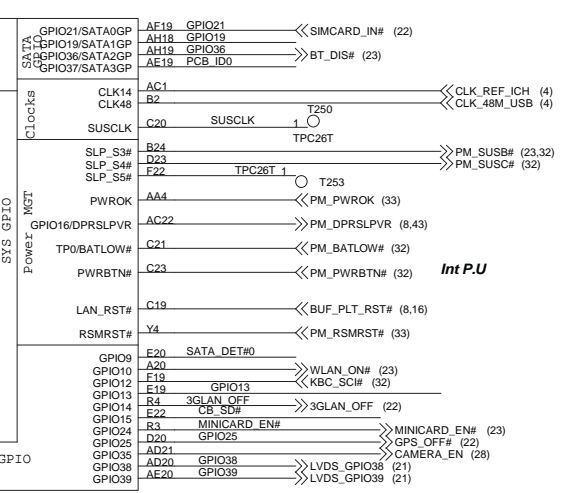
1.0G

Date: Tuesday, August 12, 2008

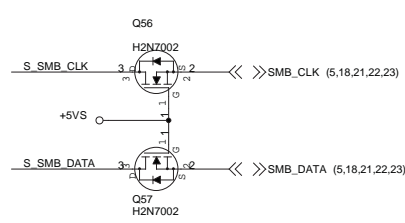
Sheet 16 of 50



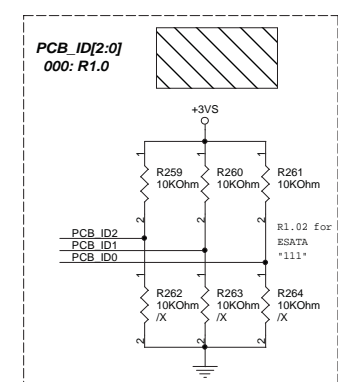
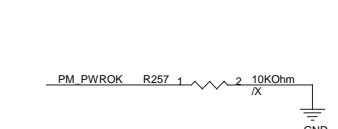
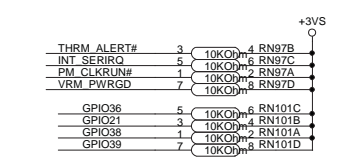
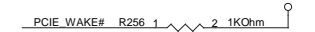
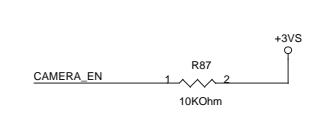
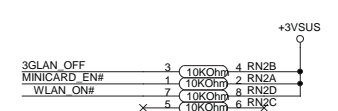
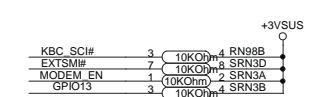
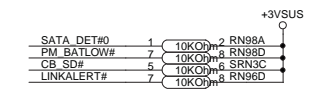
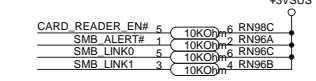
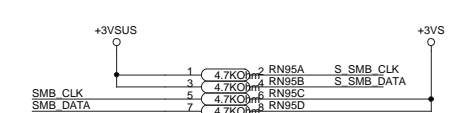
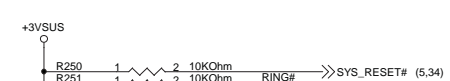
05/12/30, refer Z96J R1.01 to delete and change net name from VRMPWRGD to VRM_PWRGD.



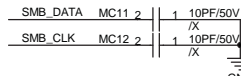
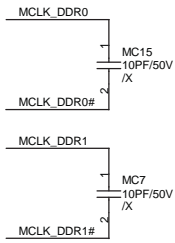
S_SMB_CLK << S_SMB_CLK (4)
S_SMB_DATA << S_SMB_DATA (4)



	WLAN_LED	WLAN	BT
High	v	v	v
High	v	x	x
High	x	v	v
Low	x	x	x



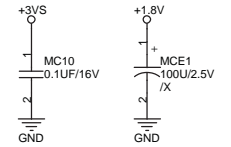
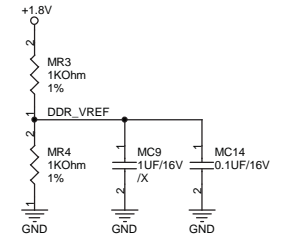
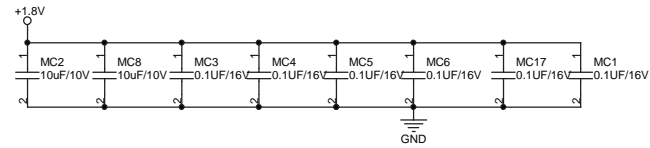
SKU	PCB_ID3 SB GPIO 19	PCB_ID2 SB GPIO 34	PCB_ID1 SB GPIO 33	PCB_ID0 SB GPIO 37
DTV	1	1	1	1
BASIC	1	1	1	0
3.5G	1	1	0	1
GPS	1	1	0	0
WiMAX	1	0	1	1
BASIC (SATA)	1	0	1	0



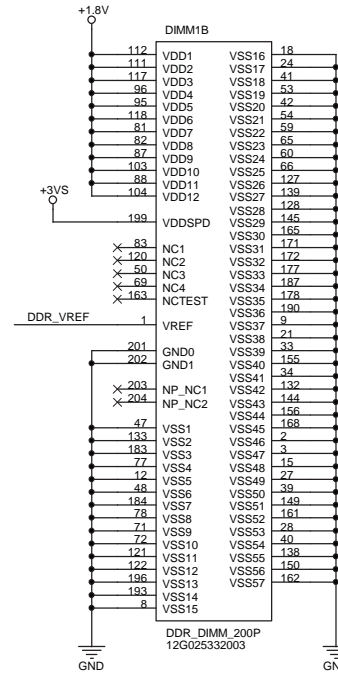
STD Type

DIMM1A			
MA_MA0	102	A0	DO0
MA_MA1	101	A1	DO1
MA_MA2	100	A2	DO2
MA_MA3	99	A3	DO3
MA_MA4	98	A4	DO4
MA_MA5	97	A5	DO5
MA_MA6	94	A6	DO6
MA_MA7	92	A7	DO7
MA_MA8	91	A8	DO8
MA_MA9	90	A9	DO9
MA_MA10	105	A10/AP	DO10
MA_MA11	90	A11	DO11
MA_MA12	89	A12	DO12
MA_MA13	116	A13	DO13
	86	A14	DO14
	84	A15	DO15
MA_BA2	85	A16_BA2	DO16
MA_BA0	107	BA0	DO17
MA_BA1	106	BA1	DO18
	110	SO#	DO19
(8,19) MA_CS#0	115	S#0	DO20
(8,19) MA_CS#1	114	S#1	DO21
(8) MCLK_DDR0	30	CK0	DO22
(8) MCLK_DDR0#	32	CK0#	DO23
(8) MCLK_DDR1	166	CK1	DO24
(8) MCLK_DDR1#	79	CK1#	DO25
(8,19) MA_CKE0	80	CKE0	DO26
(8,19) MA_CKE1	80	CKE1	DO27
(10,19) MA_CAS#	113	CAS#	DO28
(10,19) MA_RAS#	108	RAS#	DO29
(10,19) MA_WE#	109	WE#	DO30
	198	SA0	DO31
	200	SA1	DO32
(5,17,21,22,23) SMB_CLK	197	SCL	DO33
(5,17,21,22,23) SMB_DATA	195	SDA	DO34
(8,19) MA_ODT0	114	ODT0	DO35
(8,19) MA_ODT1	119	ODT1	DO36
		DM0	DO37
MA_DM0	10	DM0	DO38
MA_DM2	26	DM2	DO39
MA_DM1	52	DM1	DO40
MA_DM3	67	DM3	DO41
MA_DM4	130	DM4	DO42
MA_DM5	147	DM5	DO43
MA_DM6	170	DM6	DO44
MA_DM7	185	DM7	DO45
		MA_DQ0	DO46
MA_DQ0	13	DO46	MA_DQ0
MA_DQ0#	31	DO47	MA_DQ0#
MA_DQ1	51	DO48	MA_DQ1
MA_DQ1#	70	DO49	MA_DQ1#
MA_DQ2	131	DO50	MA_DQ2
MA_DQ2#	148	DO51	MA_DQ2#
MA_DQ3	169	DO52	MA_DQ3
MA_DQ3#	188	DO53	MA_DQ3#
MA_DQ4	11	DO54	MA_DQ4
MA_DQ4#	29	DO55	MA_DQ4#
MA_DQ5	49	DO56	MA_DQ5
MA_DQ5#	68	DO57	MA_DQ5#
MA_DQ6	129	DO58	MA_DQ6
MA_DQ6#	146	DO59	MA_DQ6#
MA_DQ7	167	DO60	MA_DQ7
MA_DQ7#	186	DO61	MA_DQ7#
		DO62	
		DO63	

DDR_DIMM_200P
12G025332003

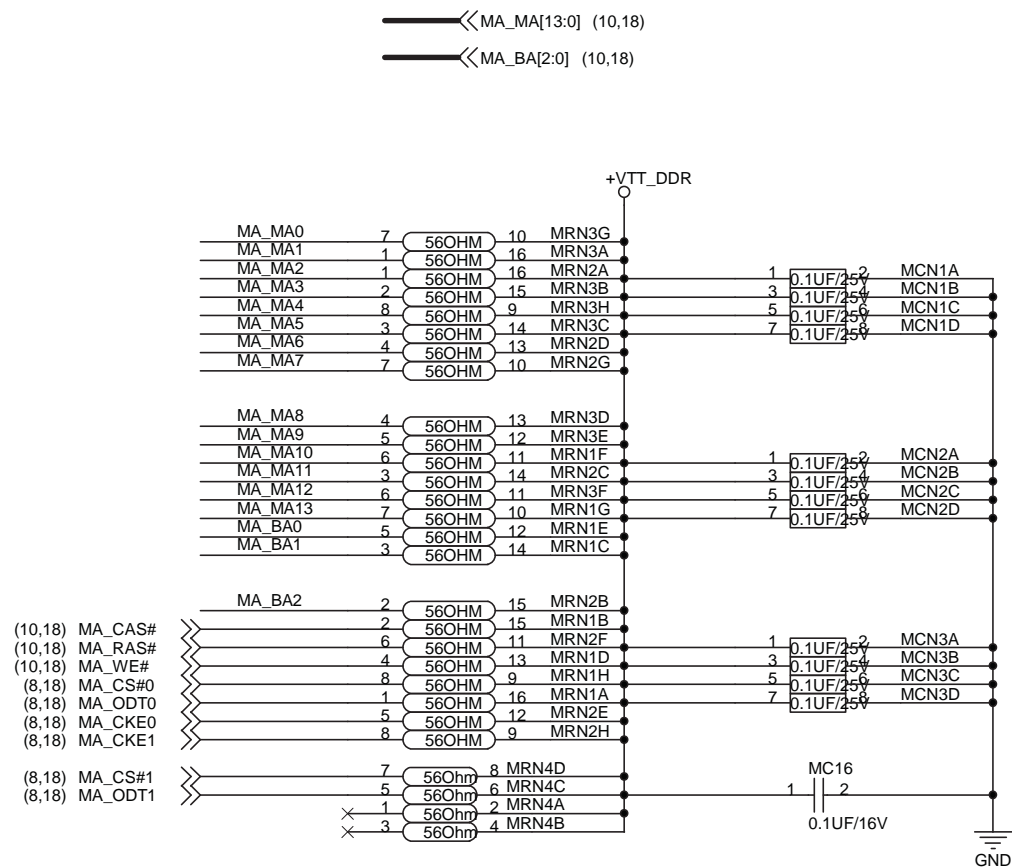


GROUP1
GROUP2
SWAP




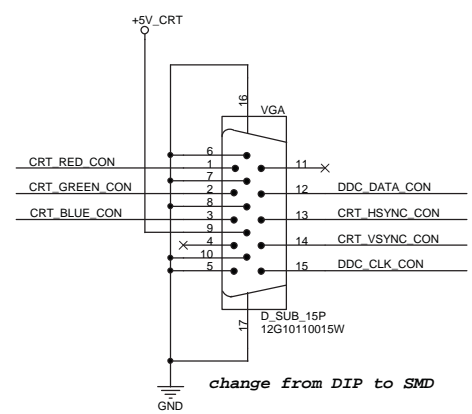
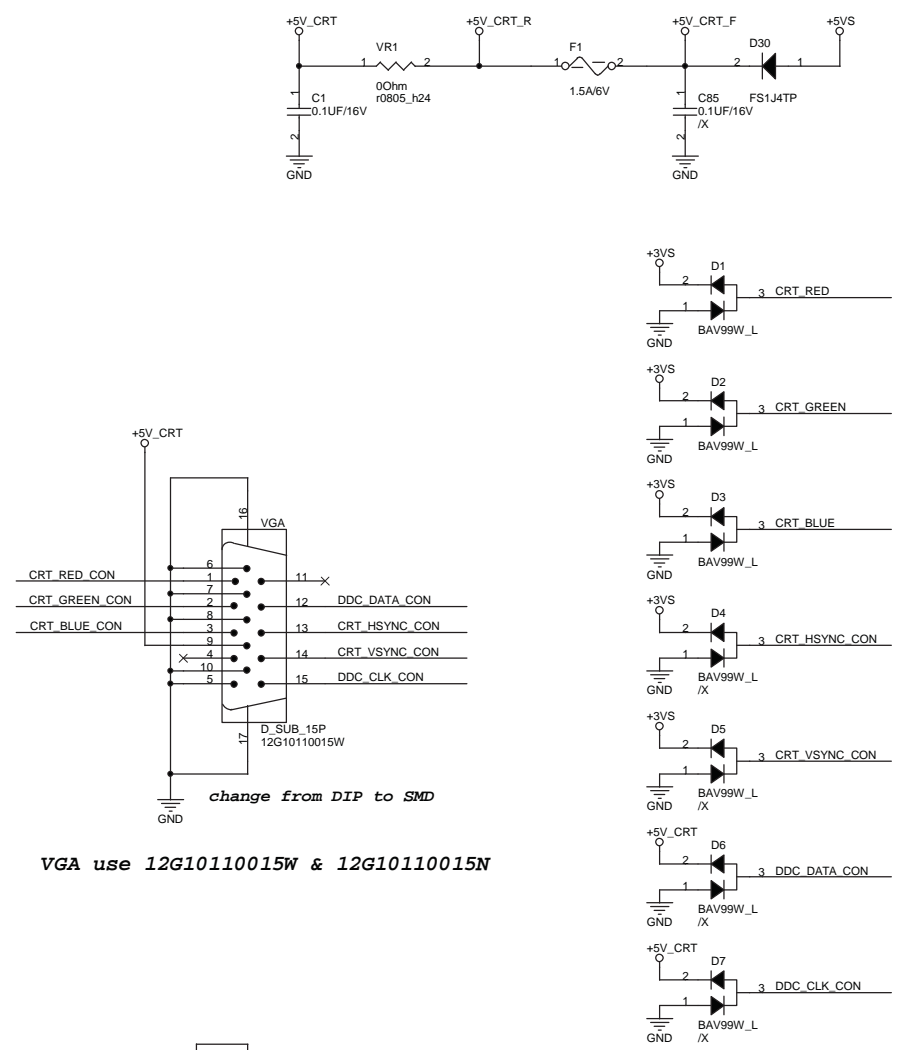
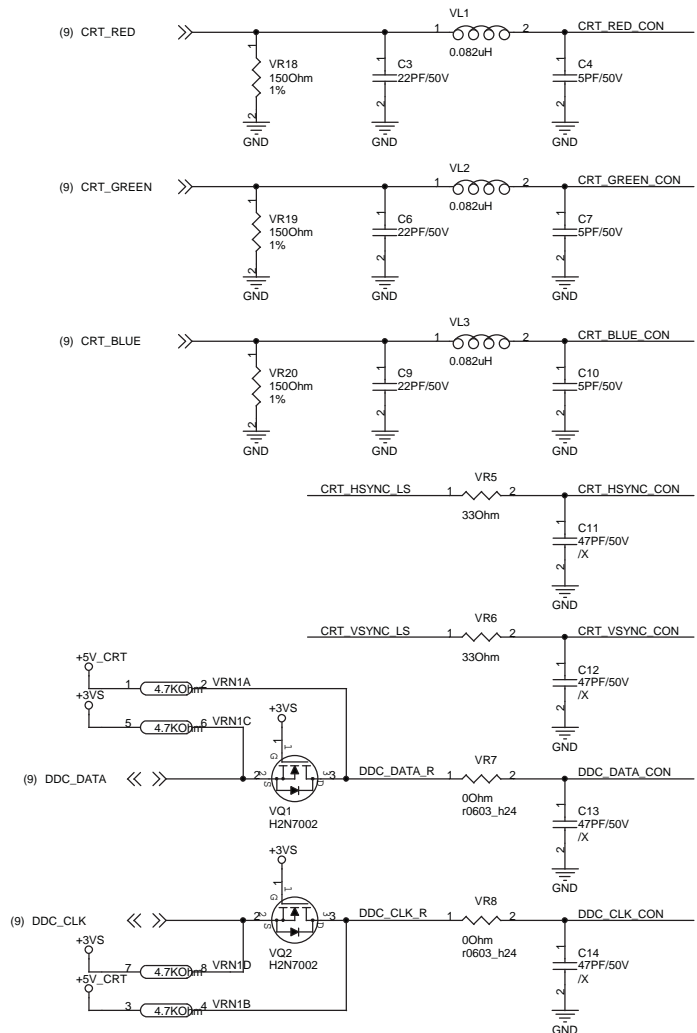
<Core Design>

ASUS		Title : DDR2 SODIMM	
ASUSTek Computer INC.		Engineer: Kell Huang	
Size A3	Project Name 1000	Rev 1.0G	
Date: Tuesday, August 12, 2008	Sheet	18	of 47

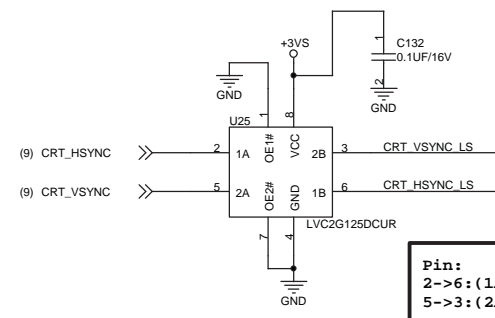


<Core Design>

		Title : DDR2_Termination	
ASUSTek Computer INC.		Engineer: Kell_Huang	
Size A4	Project Name 1000		Rev 1.0G
Date: Tuesday, August 12, 2008		Sheet 19 of 47	

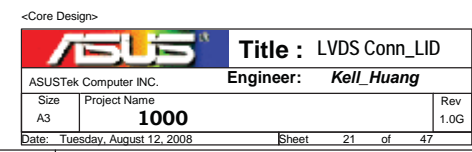


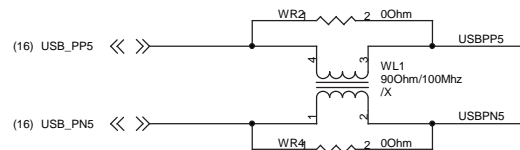
VGA use 12G10110015W & 12G10110015N



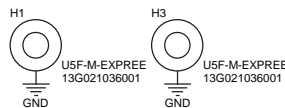
Pin:
2->6: (1A->1B)
5->3: (2A->2B)

<Core Design>		
ASUS		Title : Onboard VGA
ASUSTek Computer INC.		Engineer: Kell Huang
Size A3	Project Name 1000	Rev 1.0G
Date: Tuesday, August 12, 2008		Sheet 20 of 47



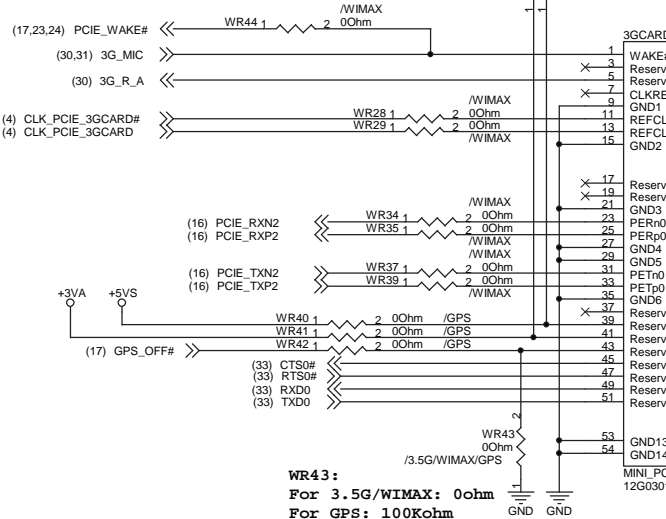
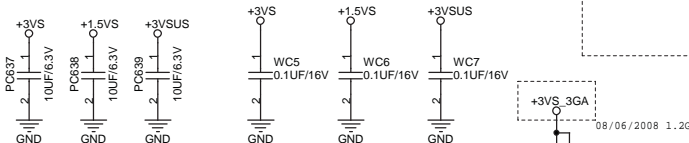
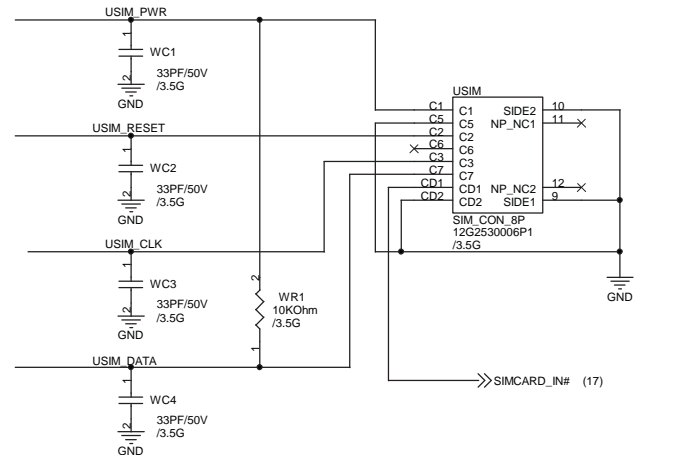


/GPS: AW GPS-M09
/DTV: ASUS MC3100U
/3.5G: SIERRA 8780
/WIMAX: INTEL5050



CAP Near SIM Socket

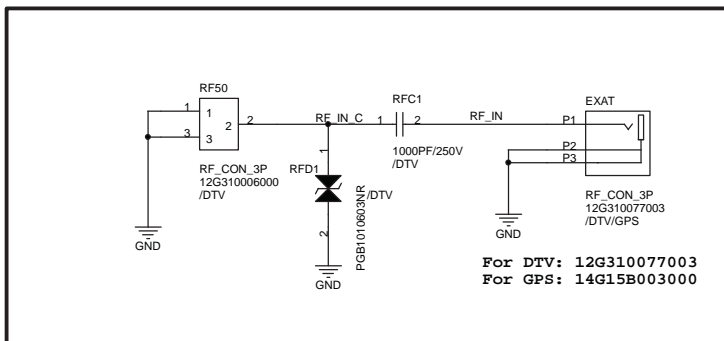
USIM_PWR (41)



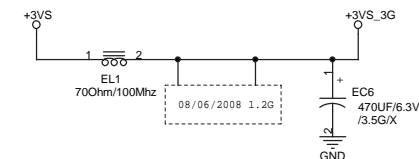
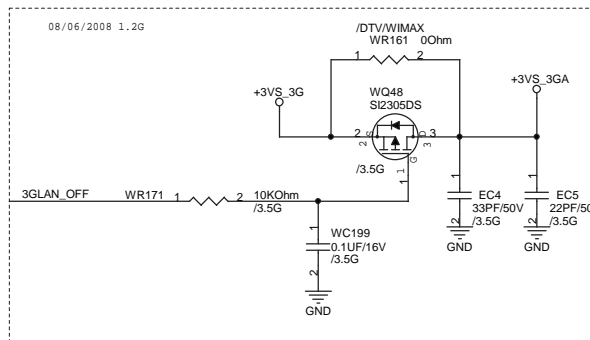
WR43:
For 3.5G/WIMAX: 0ohm
For GPS: 100Kohm

MINICARD use 12G03010052K

External Antenna



For DTV: 12G310077003
For GPS: 14G15B003000

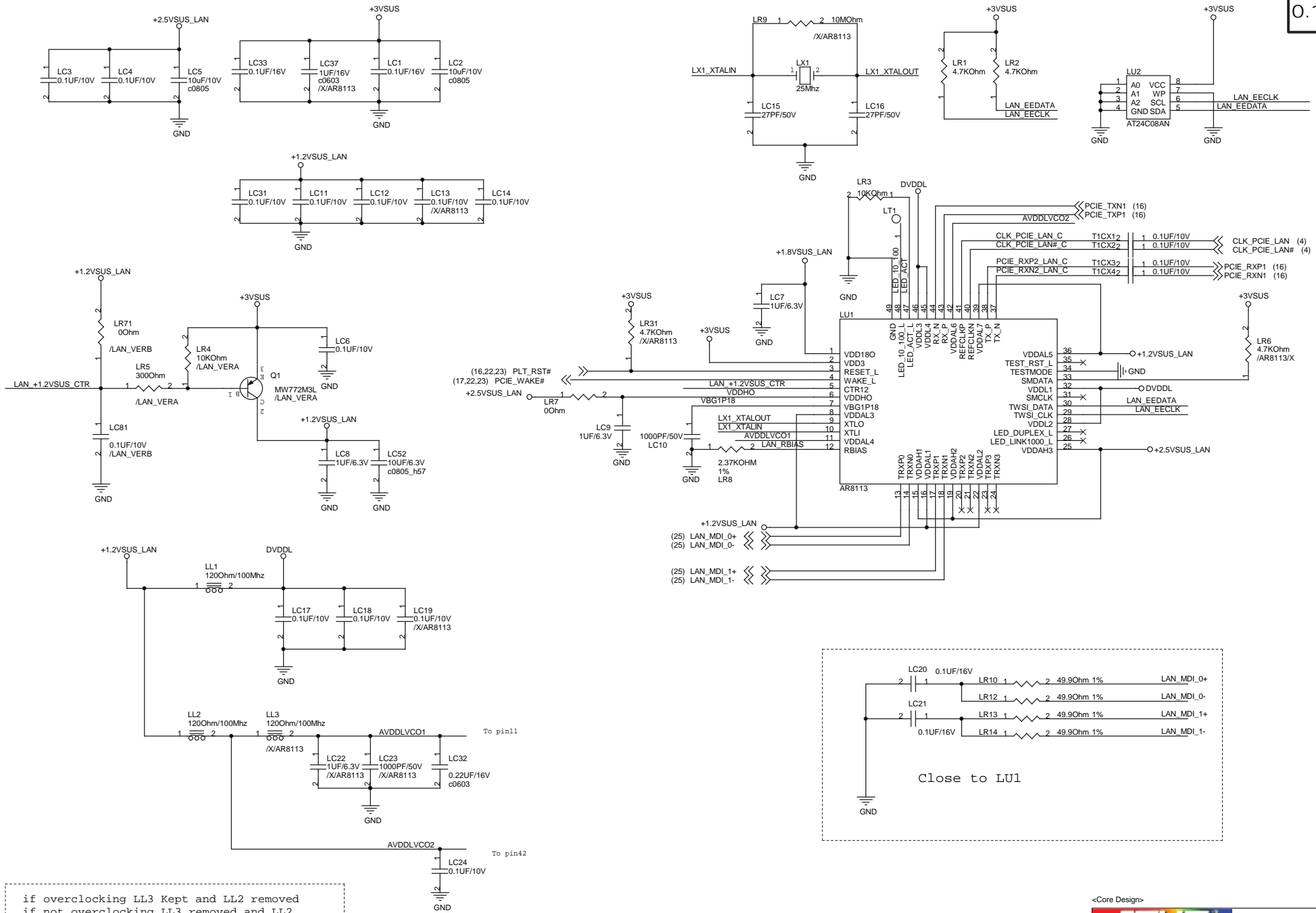


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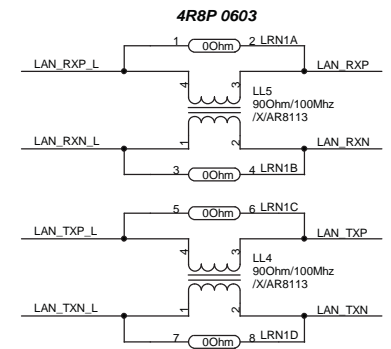
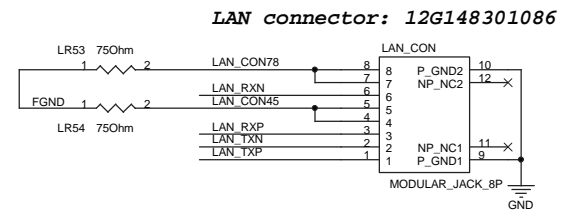
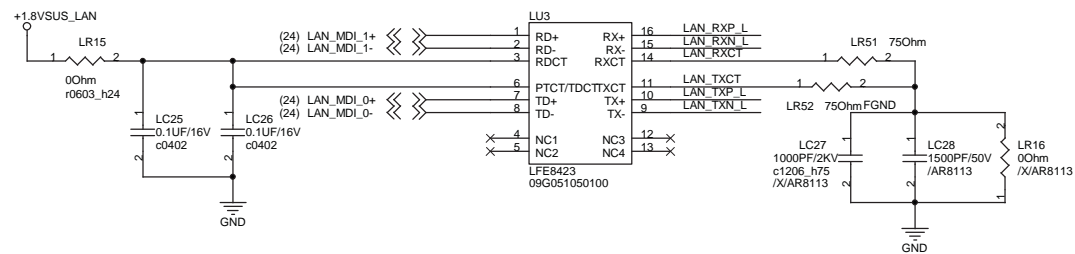
3.5G Module & External Antenna

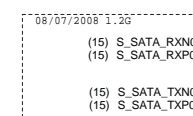
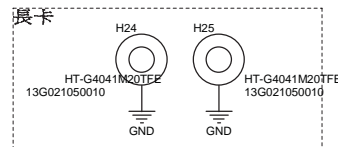
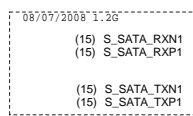
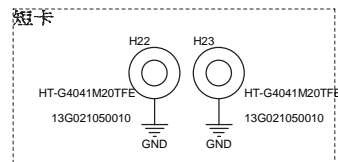
ASUS		Title :	
ASUSTek Computer INC.		Engineer: Kell_Huang	
Size	Project Name	Rev	
A3	1000	1.0G	
Date: Tuesday, August 12, 2008		Sheet 22 of 47	

0.1A Beta

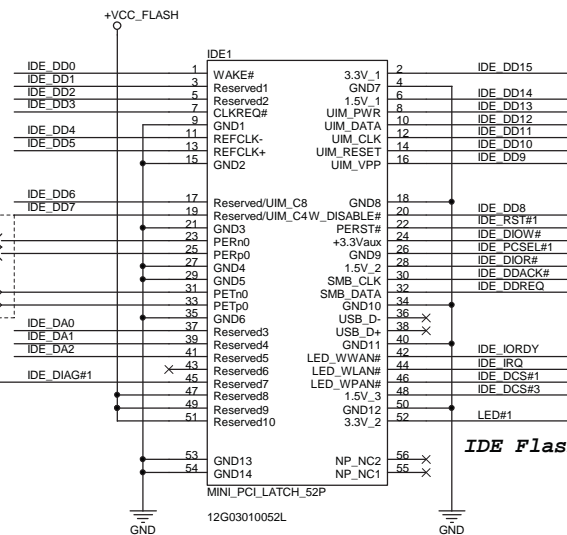
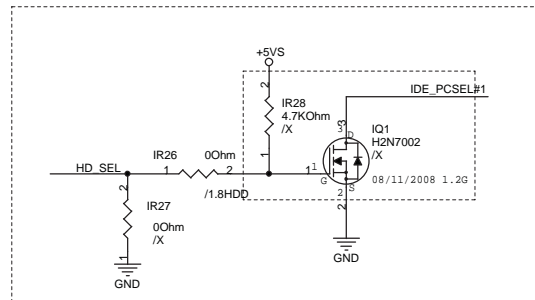


<Core Design>		ASUS		Title : AR8113	
ASUSTek Computer INC		Engineer:		Jenen_wang	
Size	Project Name	Rev		1.0G	
A3	1000				
Date:	Tuesday, August 12, 2008	Sheet	24	of	50

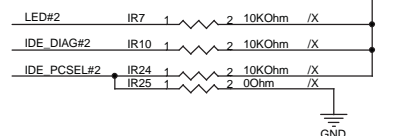
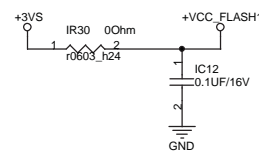
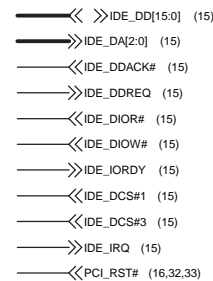




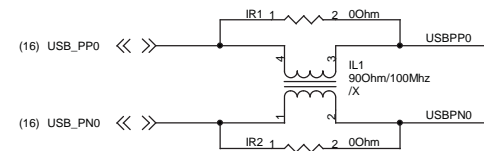
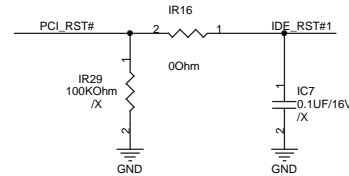
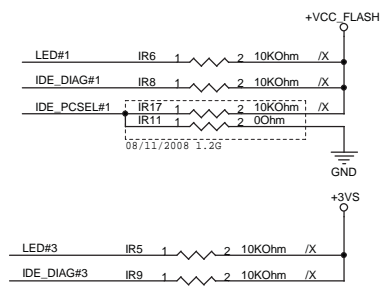
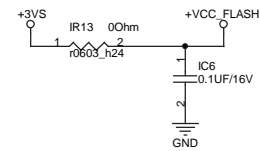
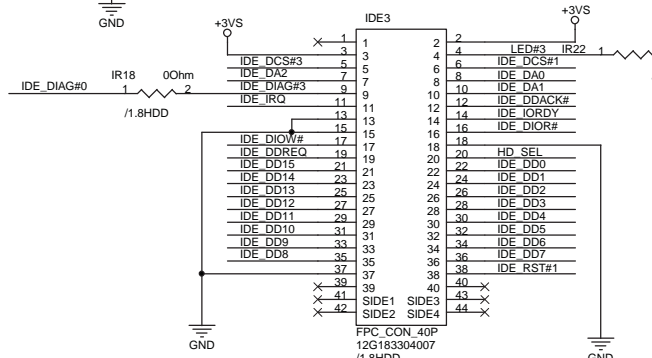
HD Master/Slave:
Master:Low
Slave :NC or High
Default :High



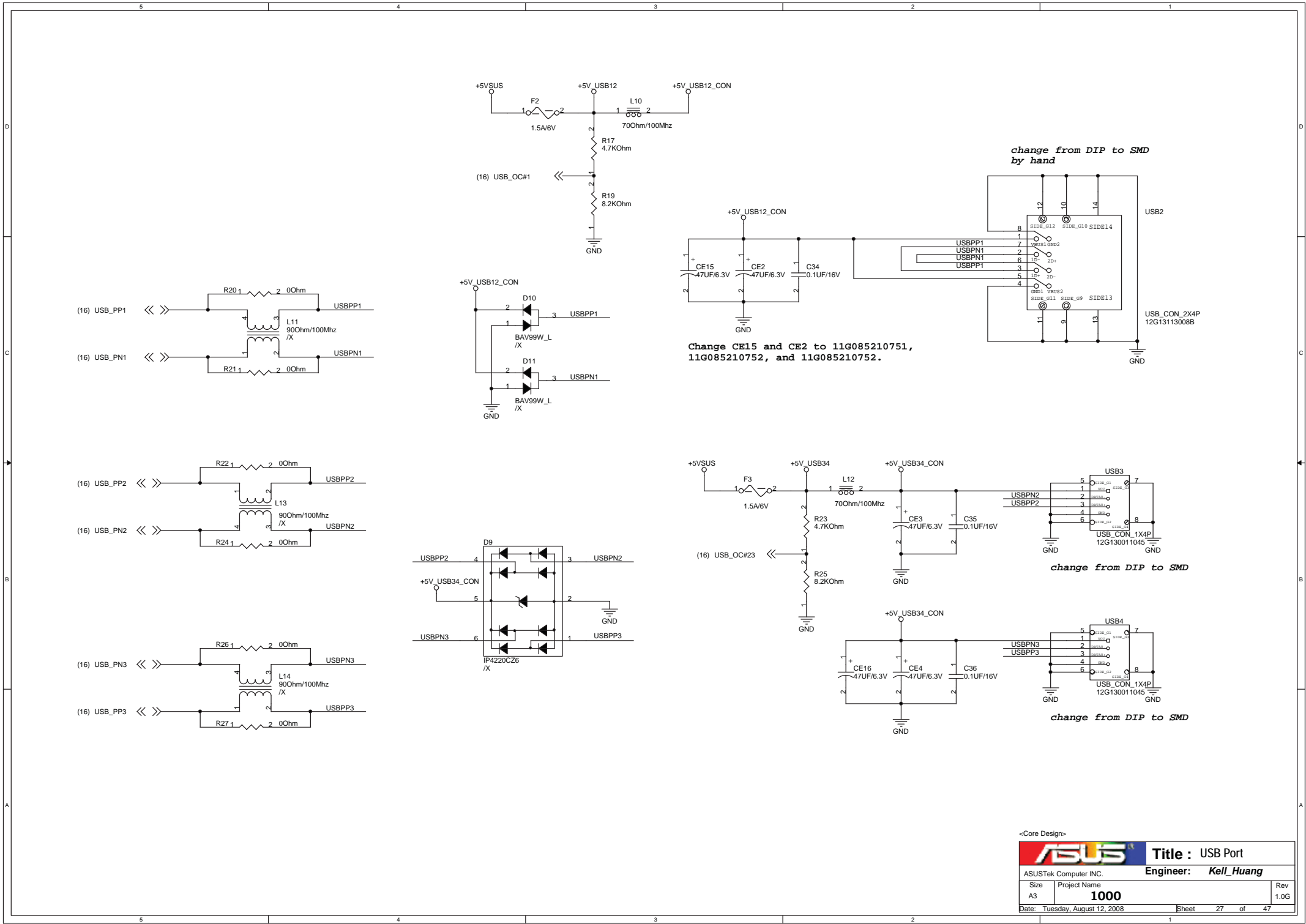
IDE Flash LED



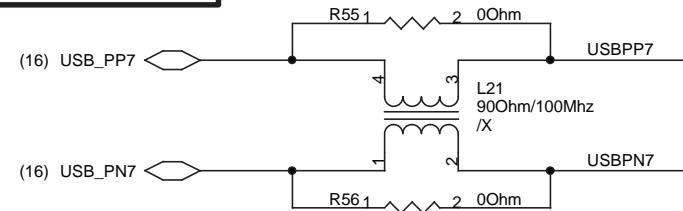
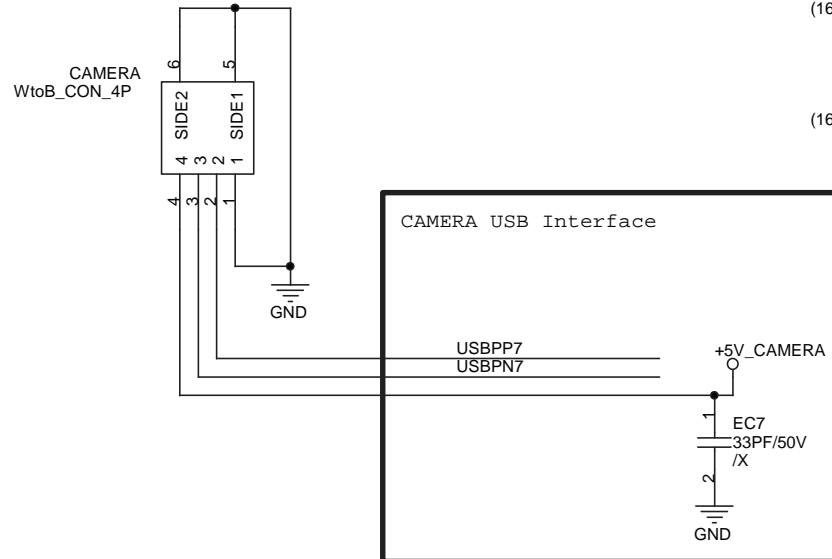
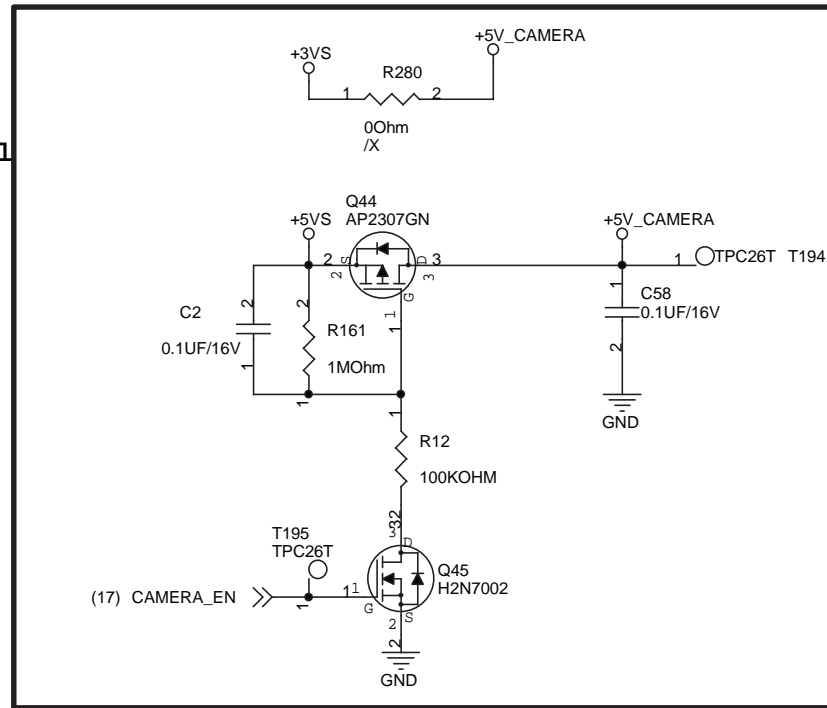
IDE Flash LED



Naming Rule:
IC:IU?
R:IR?
C:IC?
L:IL?

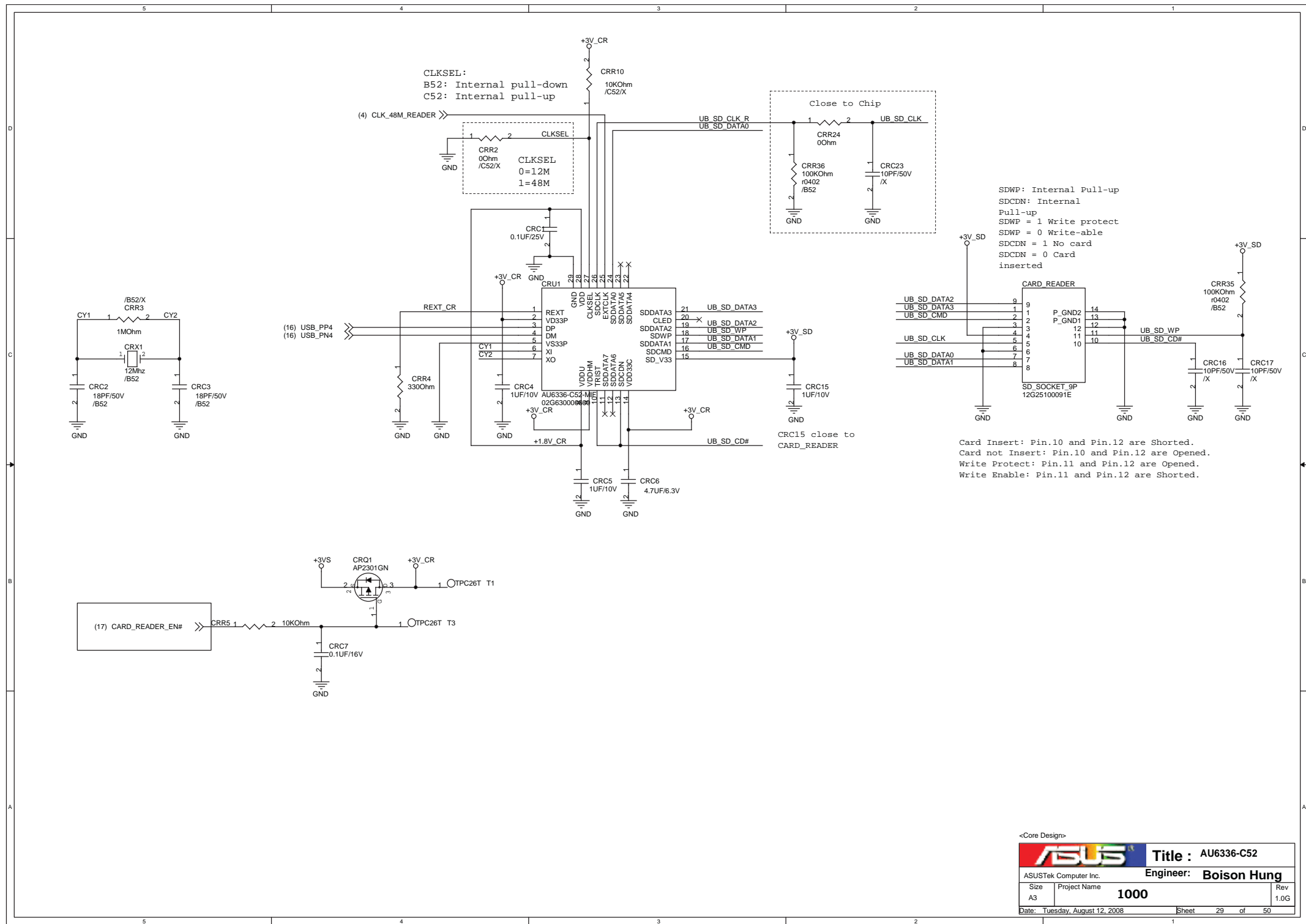


Power Control



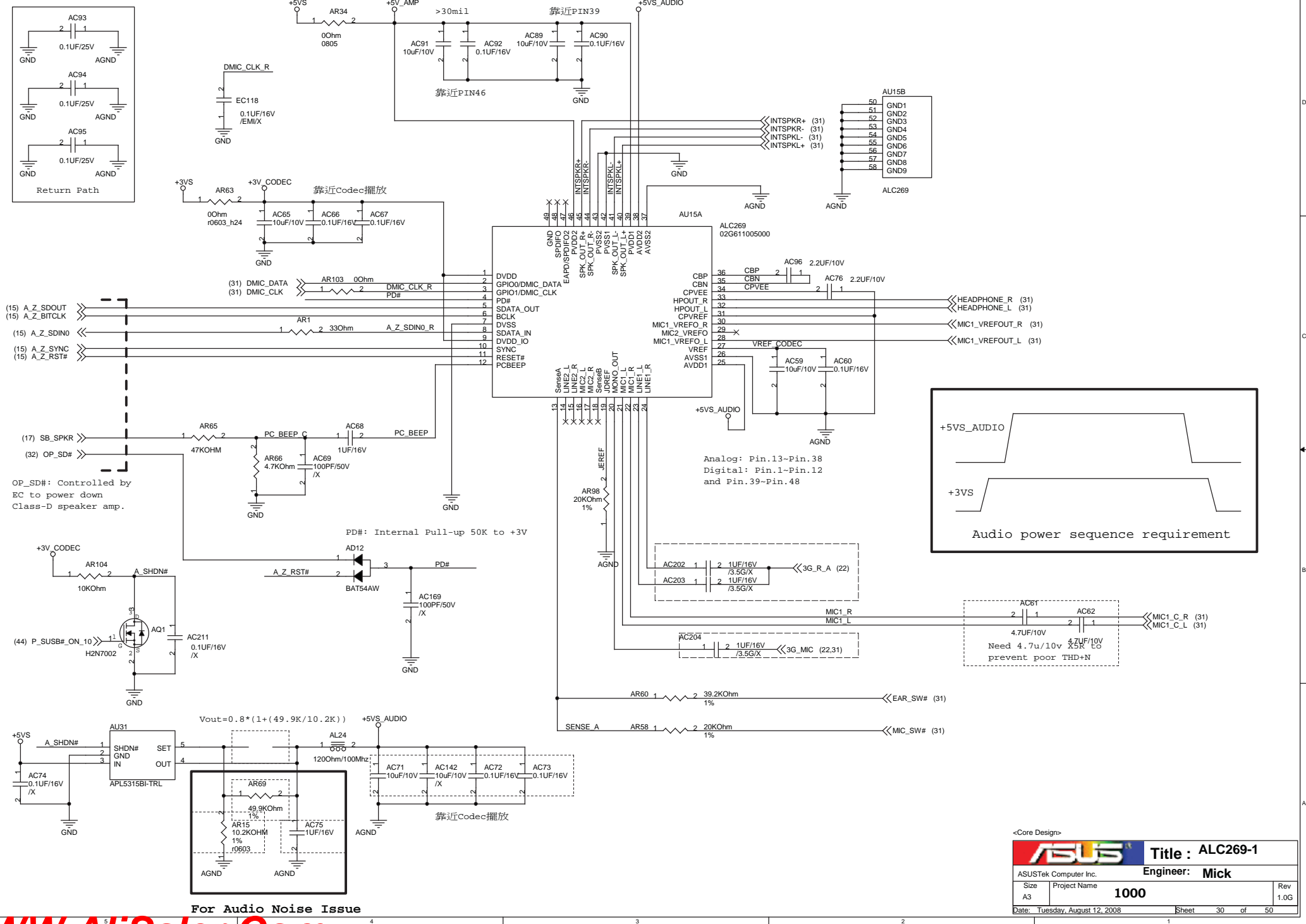
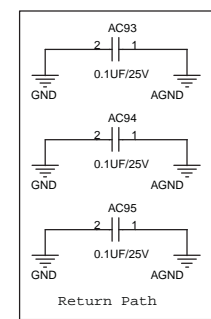
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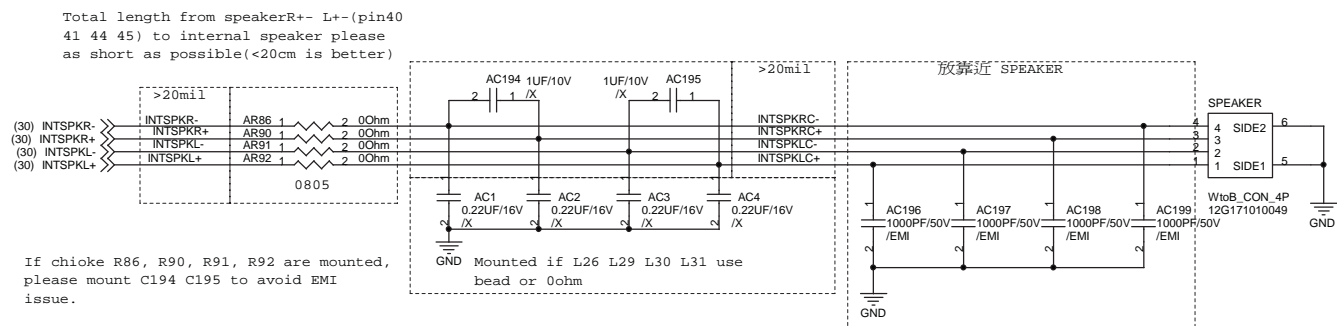
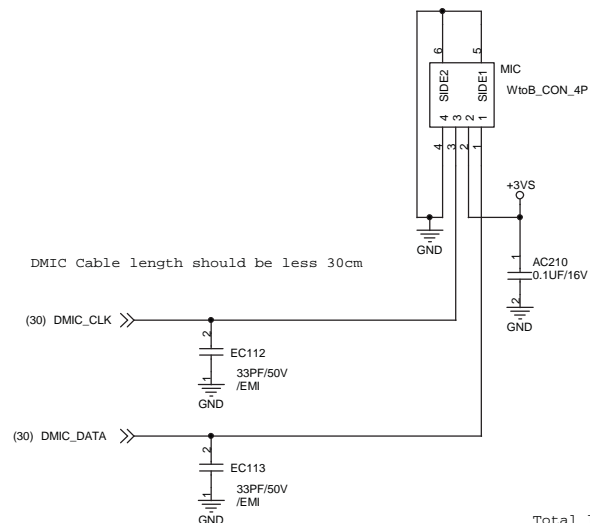
ASUS		Title : Camera Power	
ASUSTek Computer INC.		Engineer: Kell_Huang	
Size A4	Project Name 1000	Rev 1.0G	
Date: Tuesday, August 12, 2008		Sheet 28 of 47	



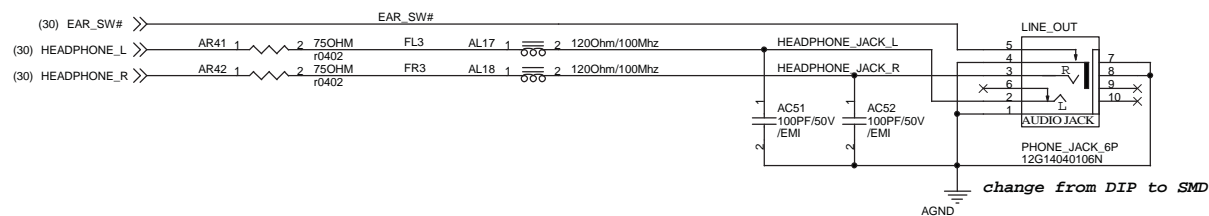
<Core Design>

ASUS		Title : AU6336-C52	
ASUSTek Computer Inc.		Engineer: Boison Hung	
Size A3	Project Name 1000	Rev 1.0G	
Date: Tuesday, August 12, 2008		Sheet 29 of 50	

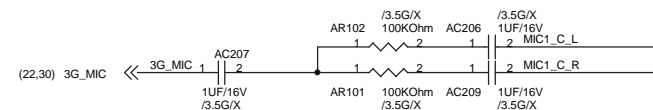
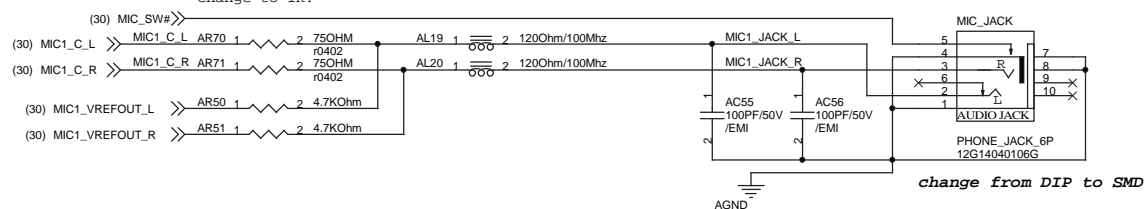




LINE_OUT use 12G14040106N

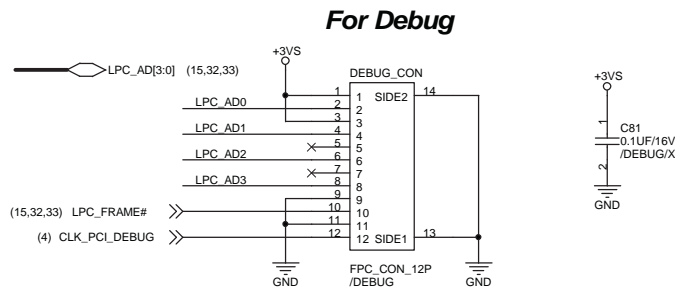
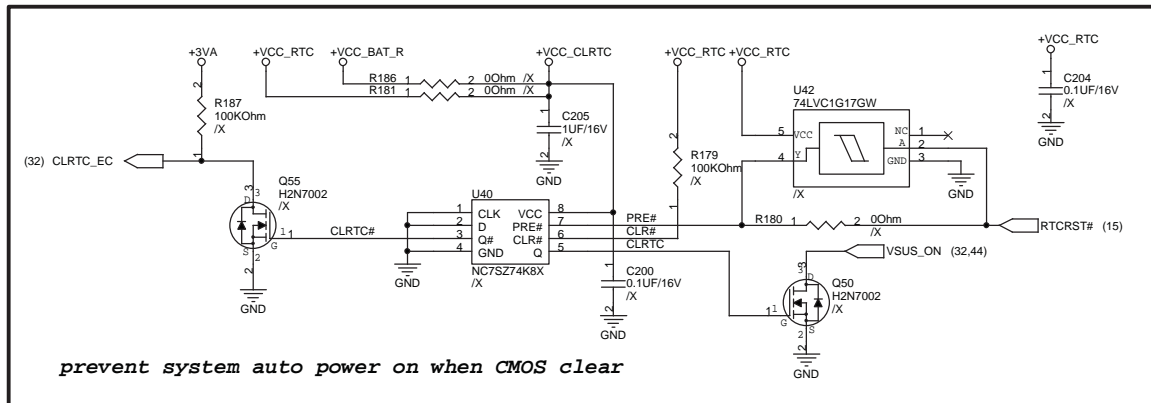
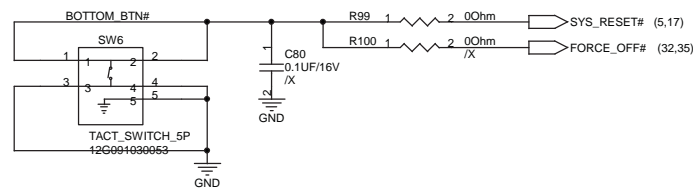
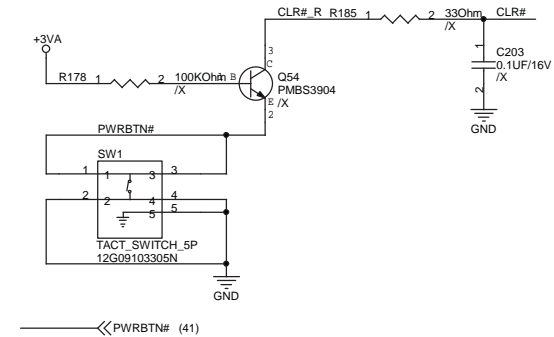
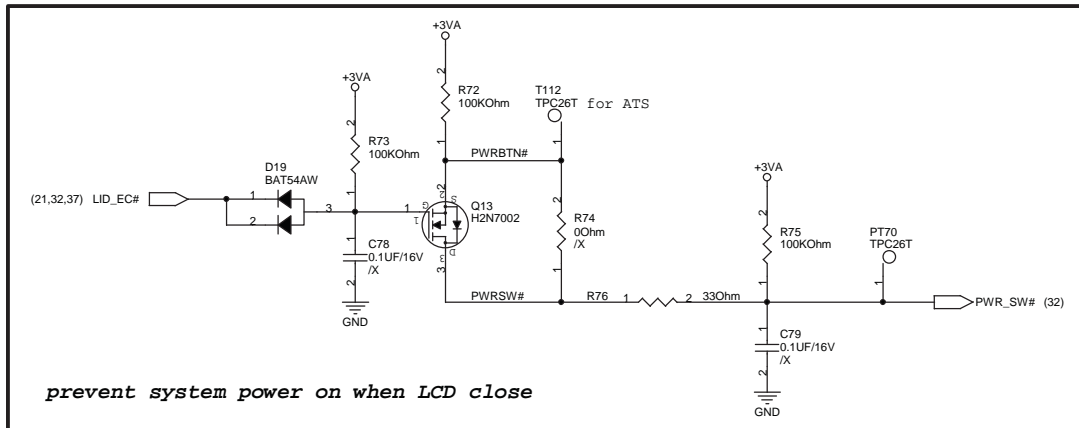


MIC_JACK use 12G14040106G

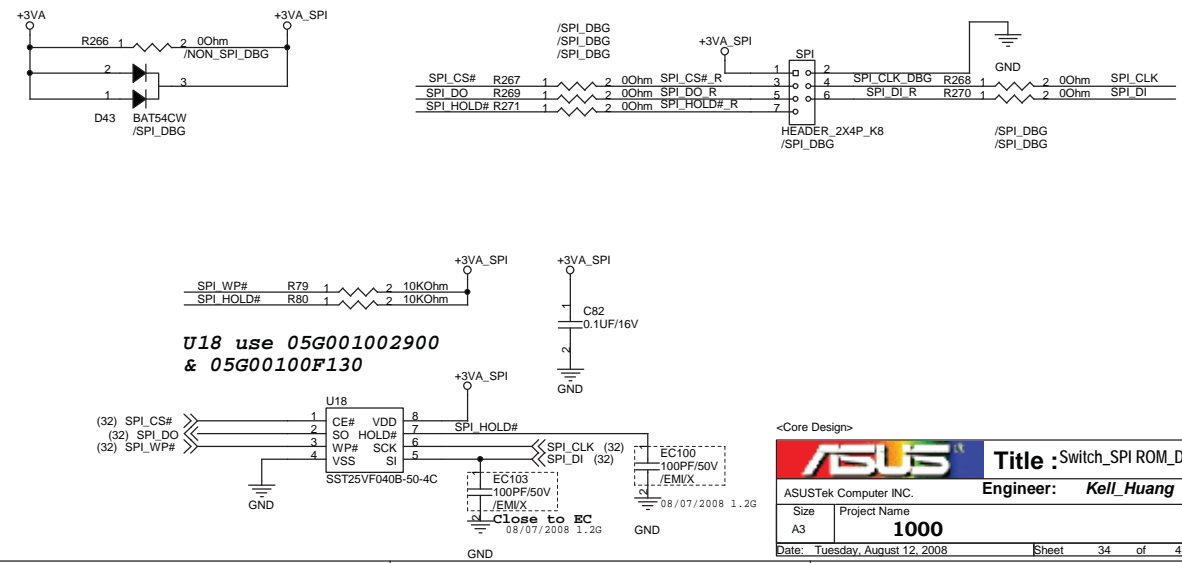




A



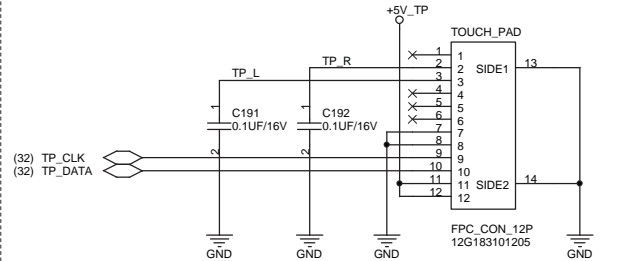
Debug Card cable use Z96 Touch Pad cable, P/N:
14G124110126, 14G124110120, 14G124110121
14G124110124, 14G124110125



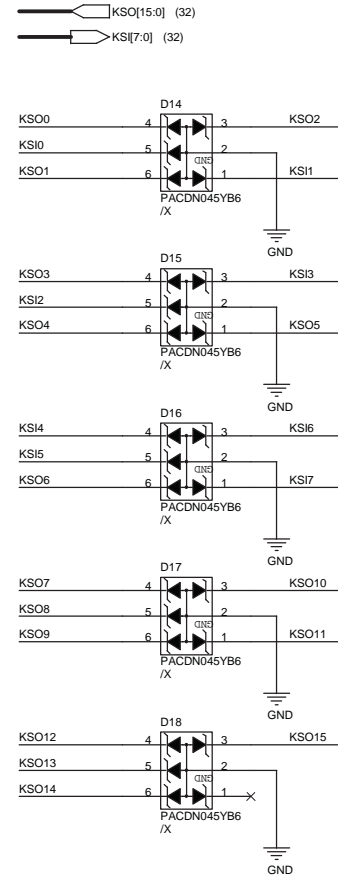
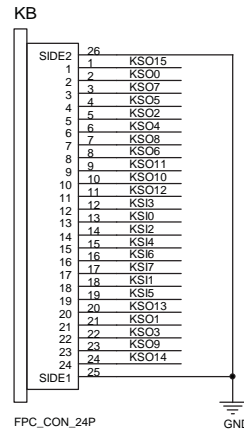
<Core Design>		
ASUS		Title : Switch_SPI ROM_Debug
ASUSTek Computer INC.		Engineer: Kell Huang
Size	Project Name	Rev
A3	1000	1.0G
Date: Tuesday, August 12, 2008		Sheet 34 of 47

For Touch-Pad

P900 R1.0G

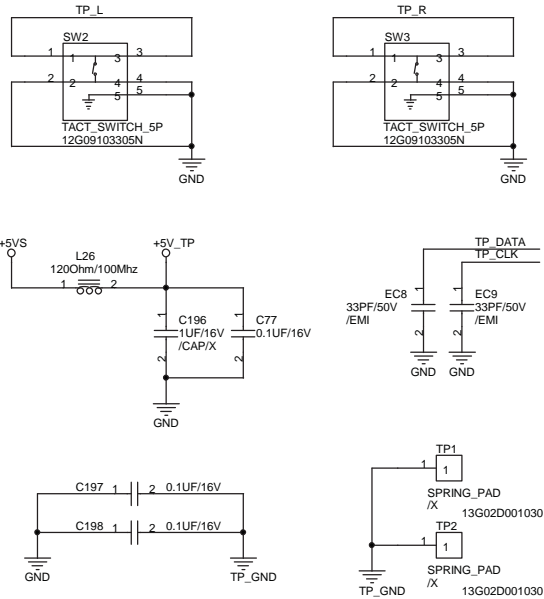


For Keyboard Connector



KSI0	EC10	1	2	33PF/50V
KSI1	EC11	1	2	33PF/50V
KSI2	EC12	1	2	33PF/50V
KSI3	EC13	1	2	33PF/50V
KSI4	EC14	1	2	33PF/50V
KSI5	EC15	1	2	33PF/50V
KSI6	EC16	1	2	33PF/50V
KSI7	EC17	1	2	33PF/50V
KSO0	EC18	1	2	33PF/50V
KSO1	EC19	1	2	33PF/50V
KSO2	EC20	1	2	33PF/50V
KSO3	EC21	1	2	33PF/50V
KSO4	EC22	1	2	33PF/50V
KSO5	EC23	1	2	33PF/50V
KSO6	EC24	1	2	33PF/50V
KSO7	EC25	1	2	33PF/50V
KSO8	EC26	1	2	33PF/50V
KSO9	EC27	1	2	33PF/50V
KSO10	EC28	1	2	33PF/50V
KSO11	EC29	1	2	33PF/50V
KSO12	EC30	1	2	33PF/50V
KSO13	EC31	1	2	33PF/50V
KSO14	EC32	1	2	33PF/50V
KSO15	EC33	1	2	33PF/50V

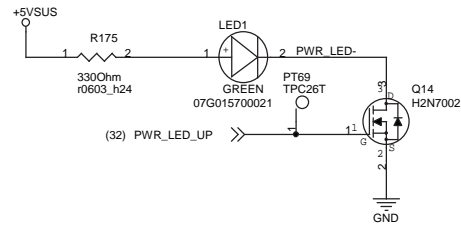
SW2, SW3 use 12G09103305N



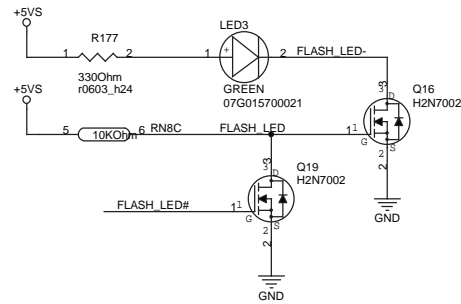
<Core Design>

ASUS		Title : KB_Touch Pad	
ASUSTek Computer INC.		Engineer: Kell_Huang	
Size A3	Project Name 1000	Rev 1.0G	
Date: Tuesday, August 12, 2008	Sheet	36	of 47

for POWER LED

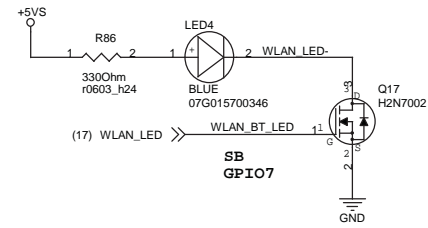


for FLASH LED

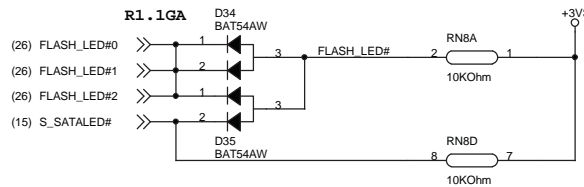
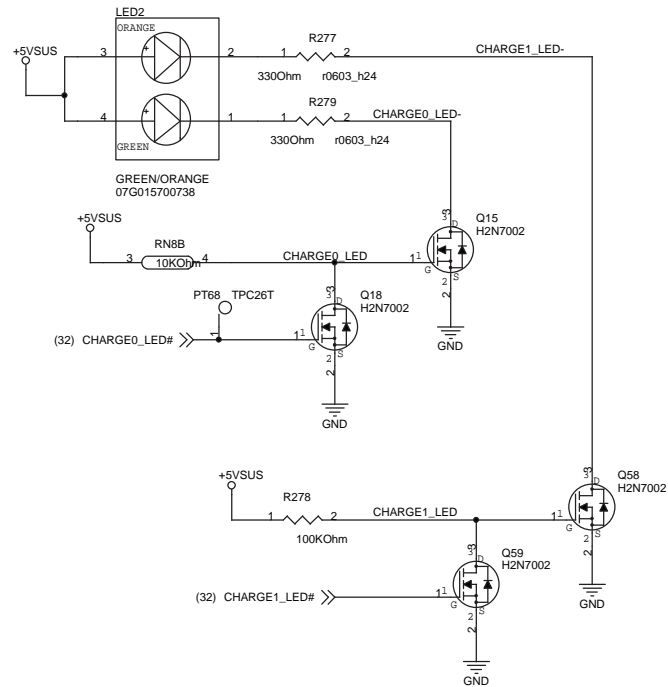


for WLAN/BlueTooth LED

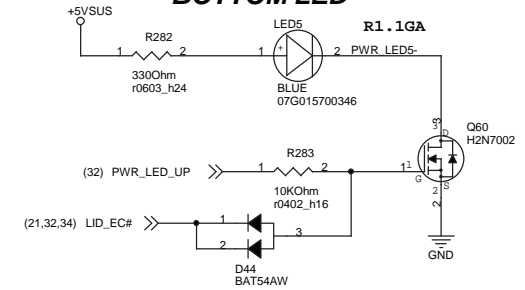
R86 use 4.7K OHm 10G213472003030



for CHARGE LED

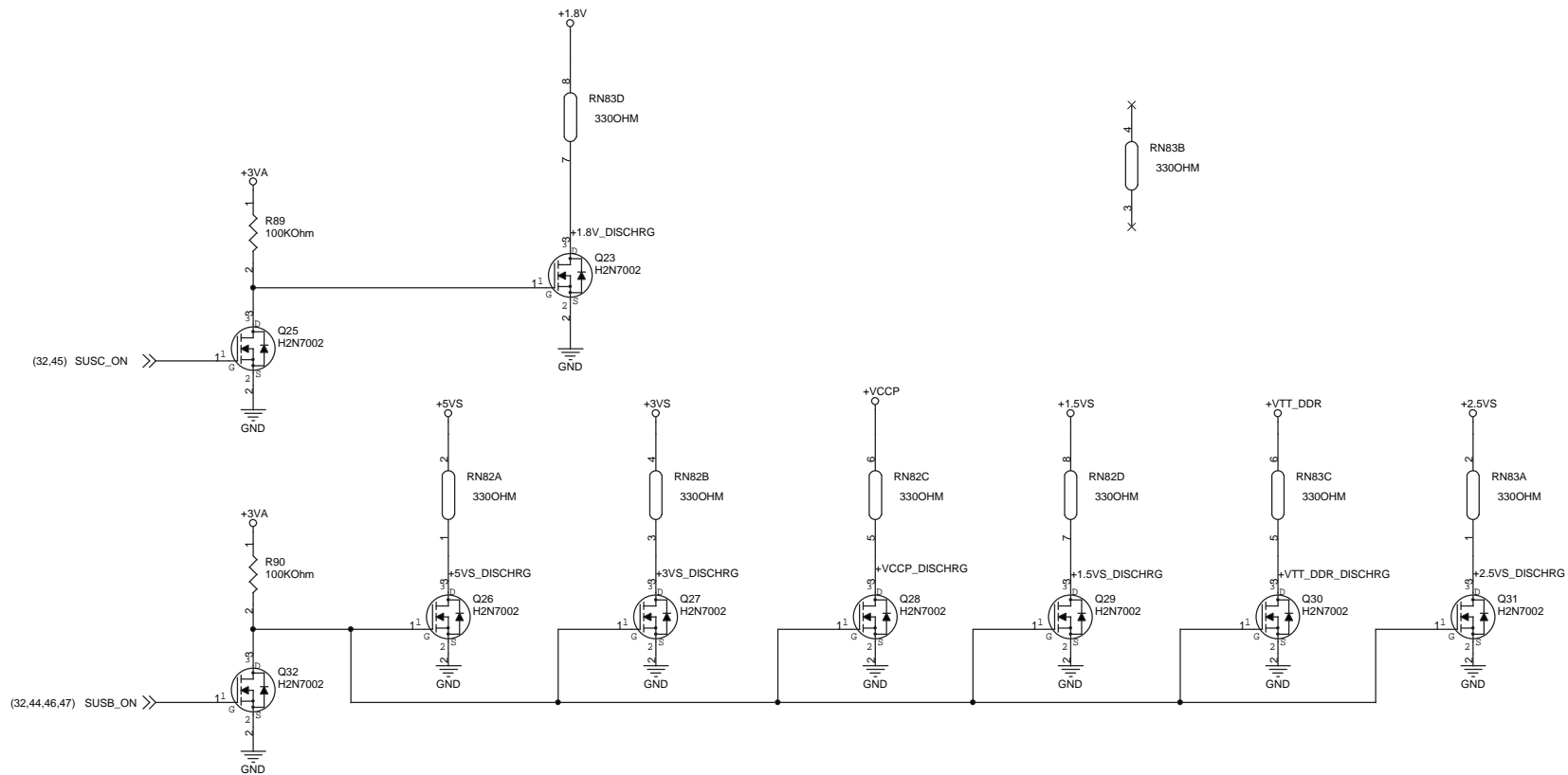


for POWER BOTTOM LED



<Core Design>

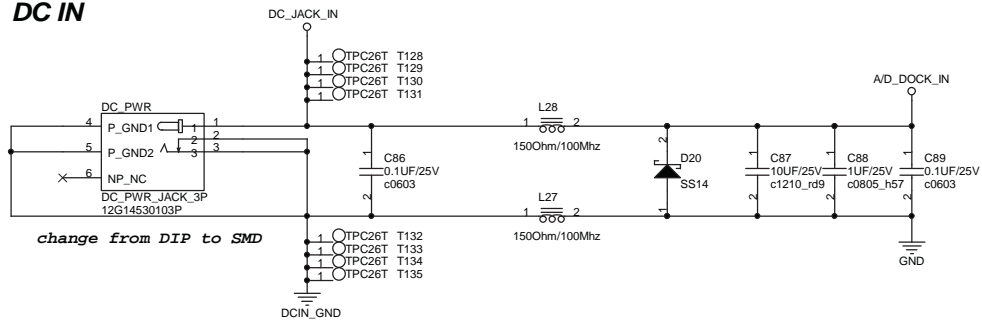
ASUS		Title : LED	
ASUSTek Computer INC.		Engineer: Kell_Huang	
Size A3	Project Name 1000	Rev 1.0G	
Date: Tuesday, August 12, 2008		Sheet 37 of 47	



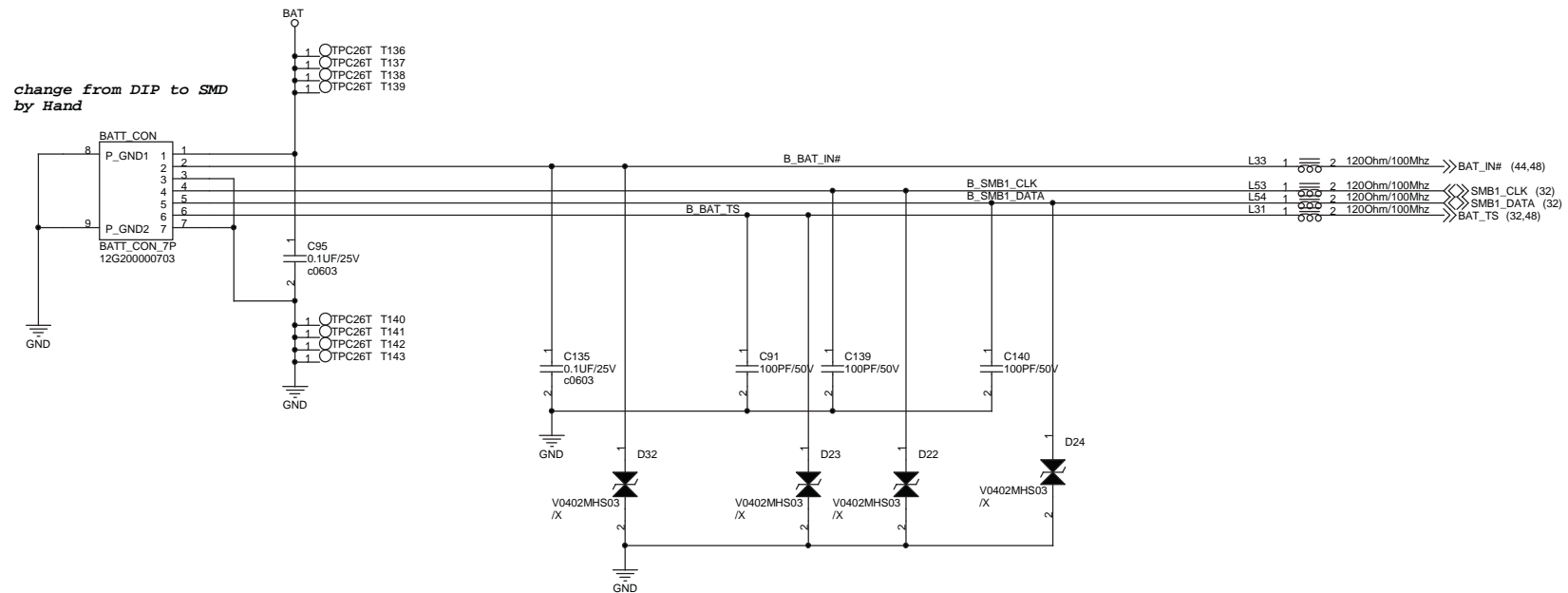
<Core Design>

ASUS		Title : Discharge	
ASUSTek Computer INC.		Engineer: Kell_Huang	
Size A3	Project Name 1000	Rev 1.0G	
Date: Tuesday, August 12, 2008	Sheet	38	of 47

DC IN

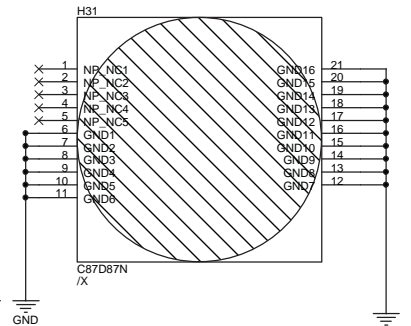
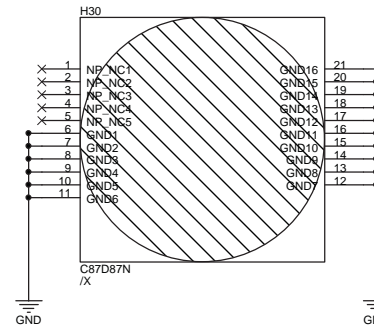
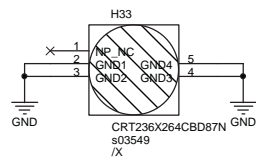
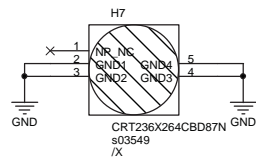
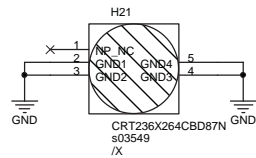
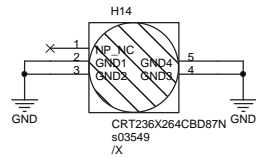
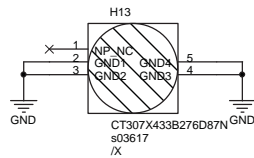
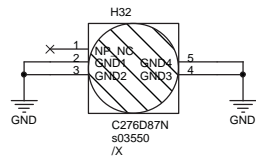
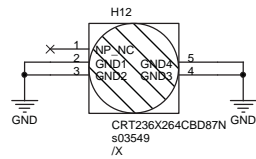
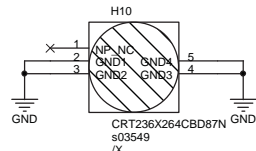
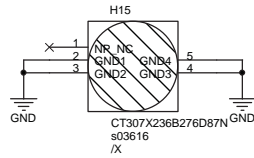
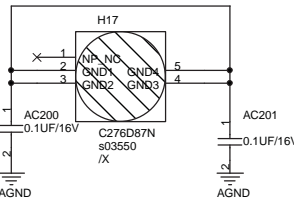
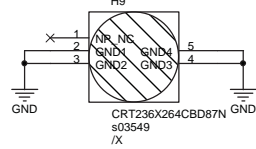
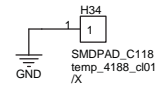
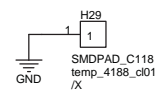
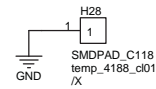
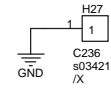
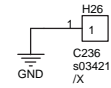
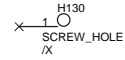
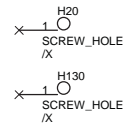
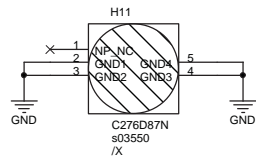
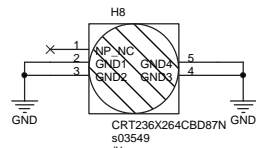


BAT IN



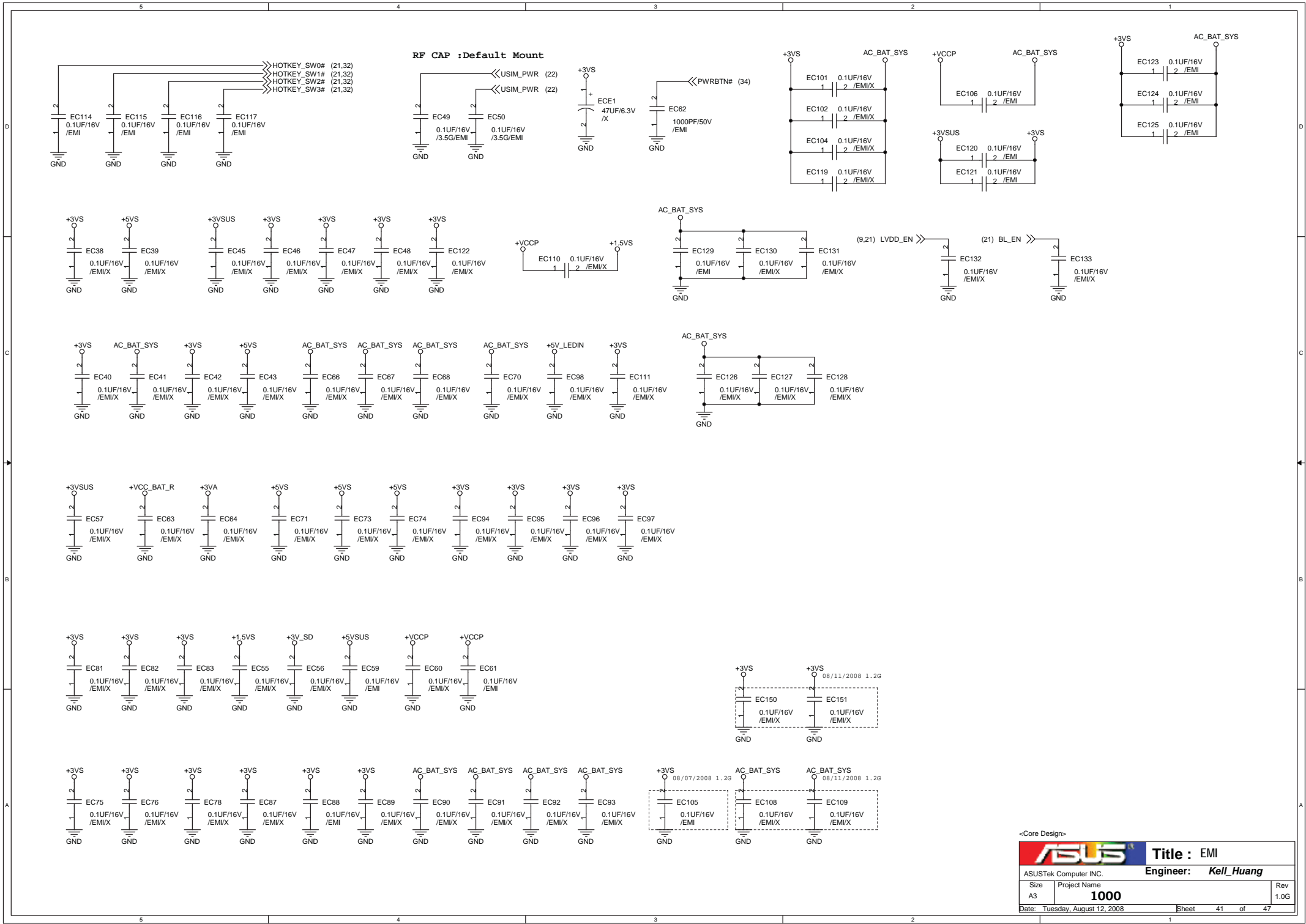
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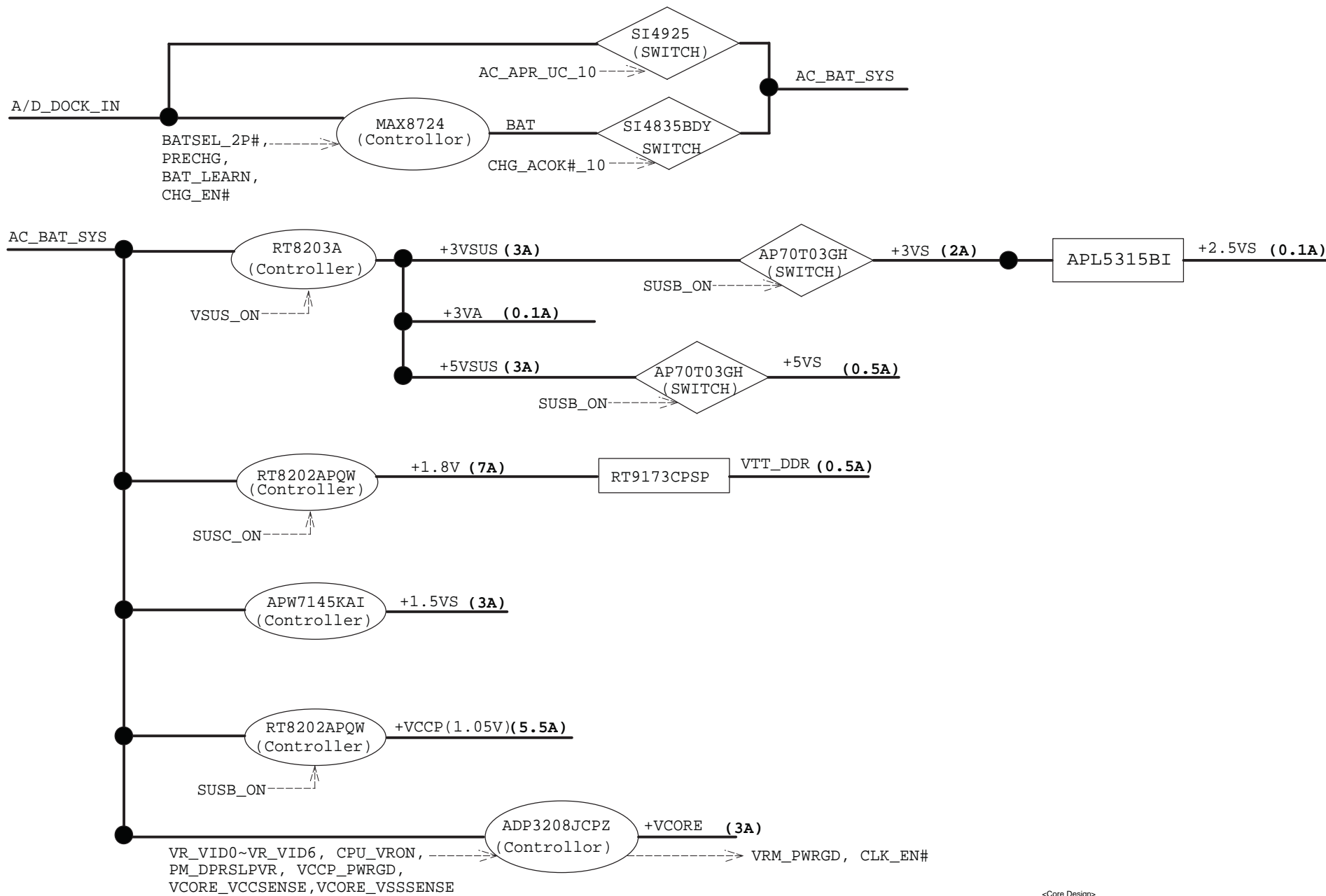
ASUS		Title : PWR Jack	
ASUSTek Computer INC.		Engineer: Kell_Huang	
Size A3	Project Name 1000	Rev 1.0G	
Date: Tuesday, August 12, 2008	Sheet	39	of 47



<Core Design>

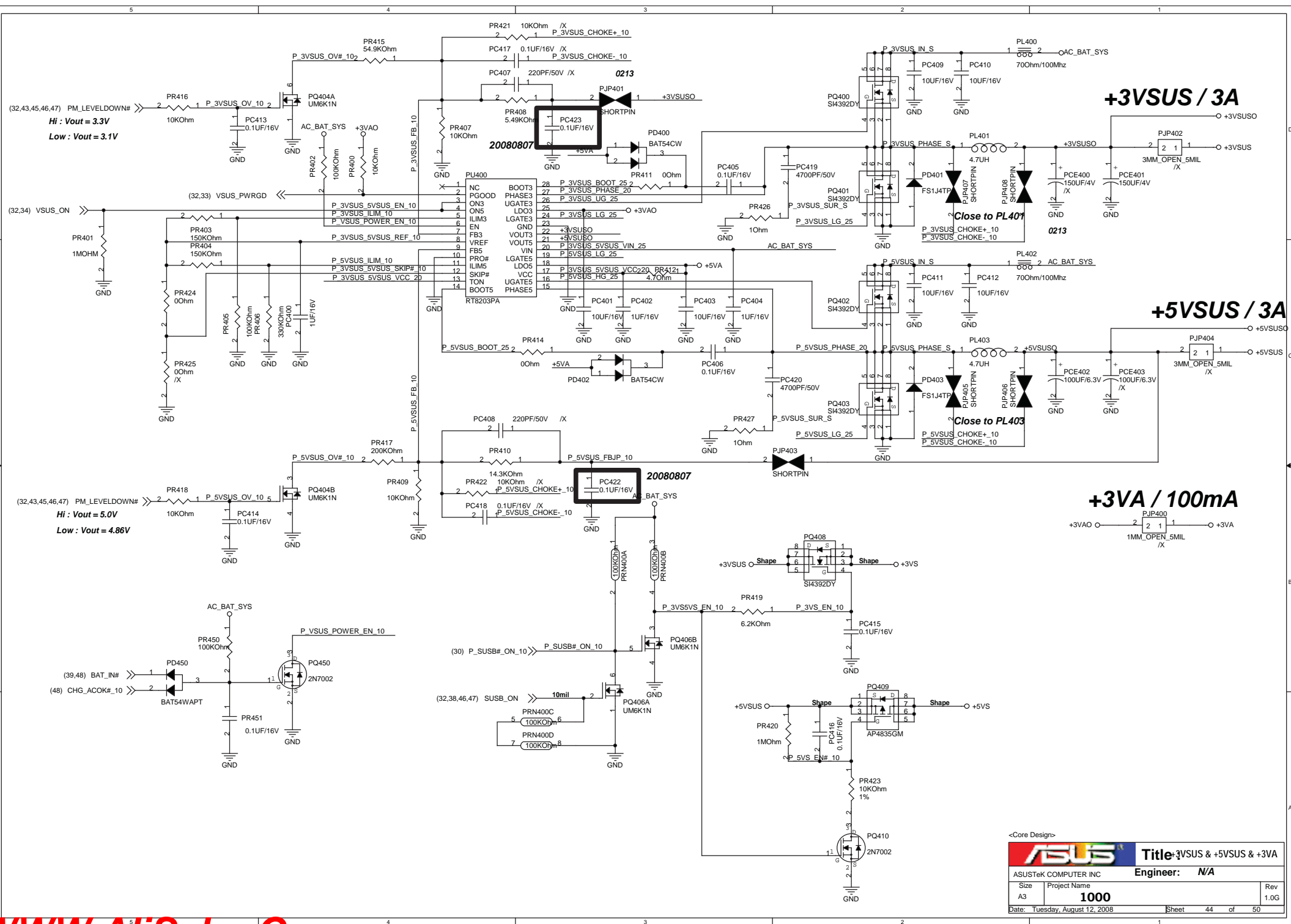
ASUS		Title : Srew Hole	
ASUSTek Computer INC.		Engineer: Kell_Huang	
Size	Project Name	Rev	
A3	1000	1.0G	
Date: Tuesday, August 12, 2008	Sheet	40	of 47





<Core Design>

ASUS		Title : Power Flow	
ASUSTek Computer INC.		Engineer: Joy_Zhou	
Size A3	Project Name 1000		Rev 1.0G
Date: Tuesday, August 12, 2008	Sheet	42 of 50	

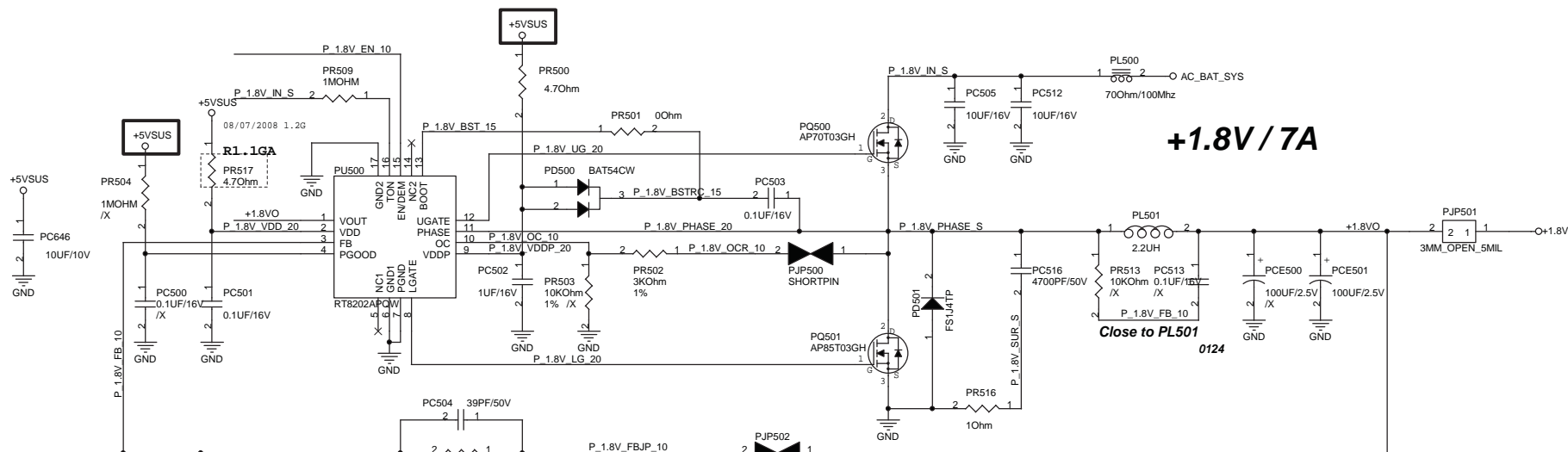


+3VSUS / 3A

+5VSUS / 3A

+3VA / 100mA

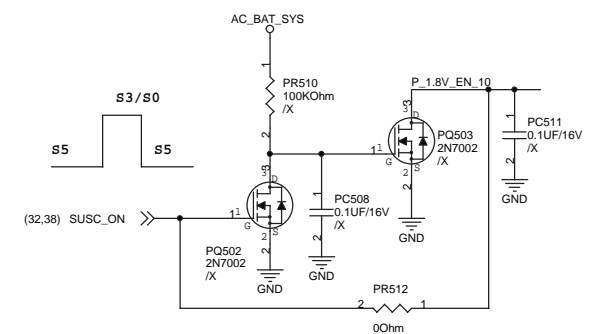
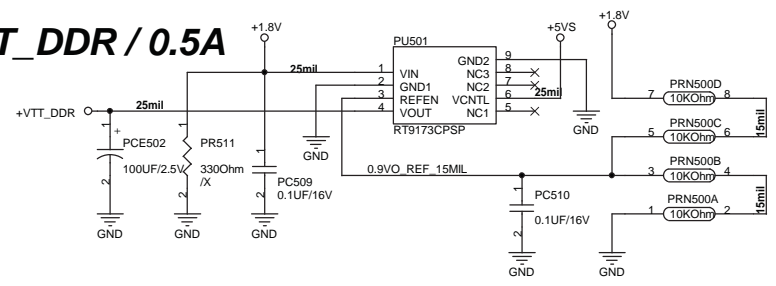
<Core Design>		Title: 3VSUS & +5VSUS & +3VA	
ASUSTek COMPUTER INC		Engineer: N/A	
Size	Project Name	Rev	
A3	1000	1.0G	
Date: Tuesday, August 12, 2008	Sheet	44	of 50



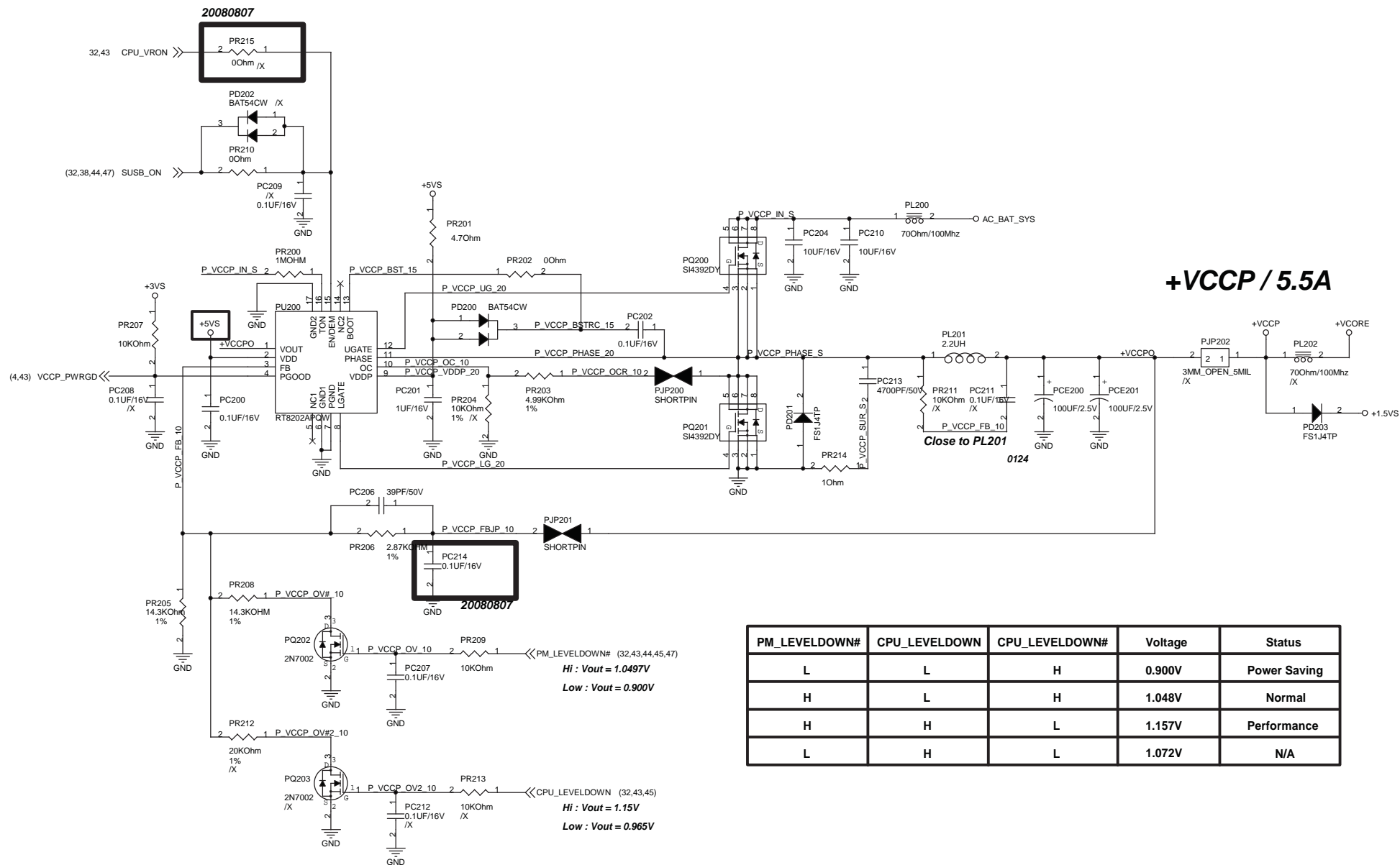
+1.8V/7A

Close to PL501
0124

VTT_DDR / 0.5A

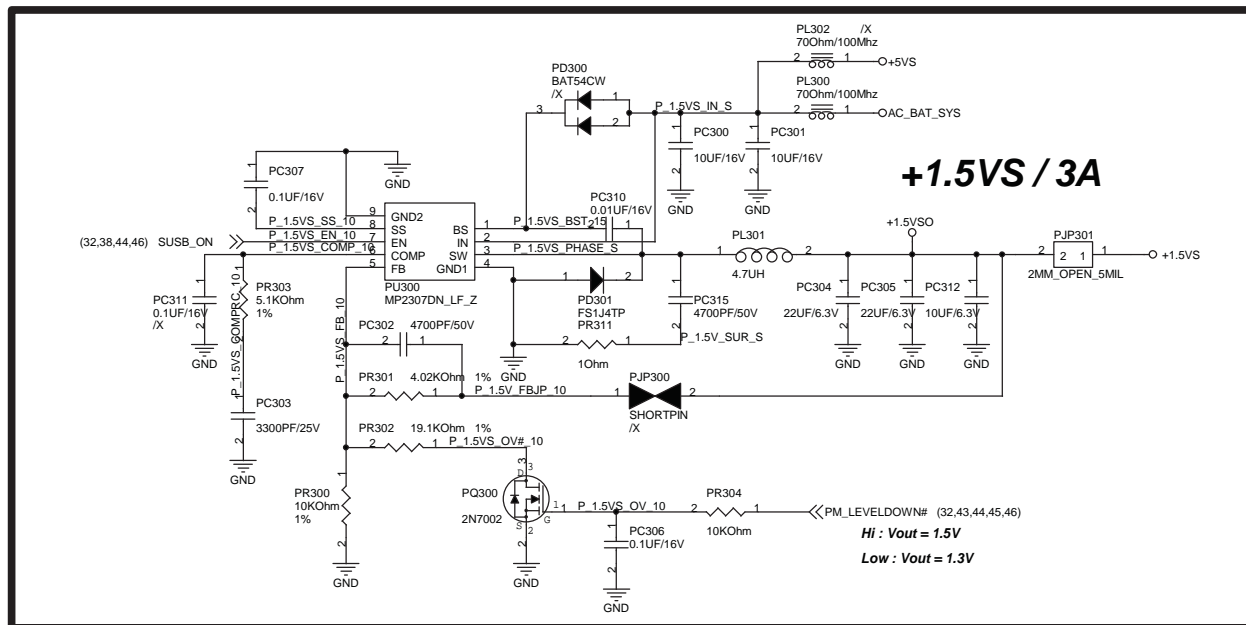


PM_LEVELDOWN#	CPU_LEVELDOWN	CPU_LEVELDOWN#	Voltage	Status
L	L	H	1.720V	Power Saving
H	L	H	1.795V	Normal
H	H	L	1.927V	Performance
L	H	L	1.782V	N/A

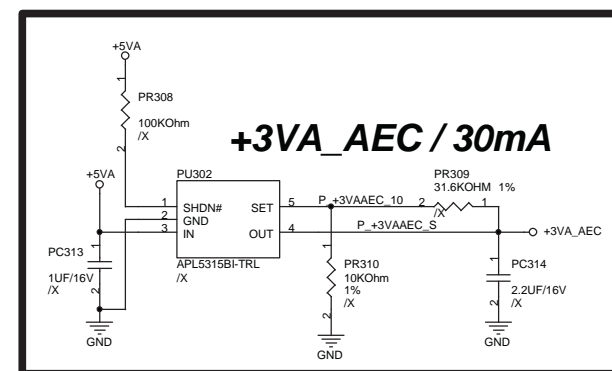
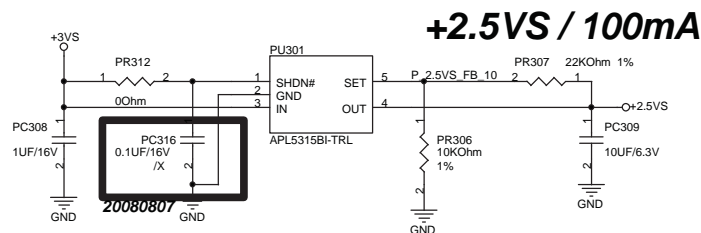


<Core Design>

ASUS		Title : VCCP	
ASUSTek Computer INC.		Engineer: Joy_Zhou	
Size A3	Project Name 1000	Rev 1.0G	
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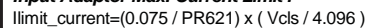
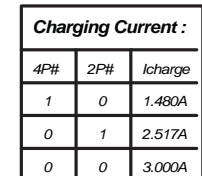


0115



<Core Design>

ASUS		Title : +1.5VS & +2.5VS	
ASUSTek Computer INC.		Engineer: Joy_Zhou	
Size	Project Name	1000	Rev 1.0G
A3			
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EC KB3310 GPIO SETTING


Pin	Pin Name	Signal Name	Type	Note
1	GPIO00/GA20	A20GATE	O	
2	GPIO01/KBRST#	RC_IN#	O	
6	GPIO04	EMAIL_SW#	I	Internal pull high
13	GPIO05/PCIRST#	PCI_RST#	I	
14	GPIO07	BAT_OTP	I	Battery over temperature
15	GPIO08	EXTSMH#	OD	10K pull high to +3VSB
16	GPIO0A	LID_EC#	I	Internal pull high
17	GPIO0B/ESB_CLK	NC	O	
18	GPIO0C/ESB_DAT	NC	O	
19	GPIO0D	DISTP_SW#	I	Internal pull high
20	GPIO0E/SC#	EXT_SC#	O	10K pull high to +3VSB
21	GPIO0F/PWM0	BL_PWM_DA	O	
23	GPIO10/PWM1	BAT_CRITICAL	I	Battery critical capacity
25	GPIO11/PWM2	PM_PWRBTN#	OD	Internal pull high in ICH
26	GPIO12/FANPWM1	FAN0_PWM	O	CPU Fan
27	GPIO13/FANPWM2	FAN1_PWM	O	VGA Fan
28	GPIO14/FANFB1	FAN0_TACH	I	CPU FanTach
29	GPIO15/FANFB2	FAN1_TACH	I	VGA FanTach
30	GPIO16/E51_TX	E51_TX	O	RS232 debug port
31	GPIO17/E51_RX	E51_RX	I	RS232 debug port
32	GPIO18	PWR_SW#	I	Internal pull high
34	GPIO19/PWM3	MAIL_LED#	O	
36	GPIO1A/NUMLED	NUM_LED#	O	
38	GPIO1D/CLKRUN#	NC	O	
39	GPIO20/KSO0/TP_TEST	KSO0	O	
40	GPIO21/KSO1/TP_PLL	KSO1	O	
41	GPIO22/KSO2	KSO2	O	
42	GPIO23/KSO3	KSO3	O	
43	GPIO24/KSO4	KSO4	O	
44	GPIO25/KSO5	KSO5	O	
45	GPIO26/KSO6	KSO6	O	
46	GPIO27/KSO7	KSO7	O	
47	GPIO28/KSO8	KSO8	O	
48	GPIO29/KSO9	KSO9	O	
49	GPIO2A/KSO10	KSO10	O	
50	GPIO2B/KSO11	KSO11	O	
51	GPIO2C/KSO12	KSO12	O	
52	GPIO2D/KSO13	KSO13	O	
53	GPIO2E/KSO14	KSO14	O	
54	GPIO2F/KSO15	KSO15	O	
55	GPIO30/KSI0	KSI0	I	Internal pull high
56	GPIO31/KSI1	KSI1	I	Internal pull high
57	GPIO32/KSI2	KSI2	I	Internal pull high
58	GPIO33/KSI3	KSI3	I	Internal pull high
59	GPIO34/KSI4	KSI4	I	Internal pull high
60	GPIO35/KSI5	KSI5	I	Internal pull high
61	GPIO36/KSI6	KSI6	I	Internal pull high
62	GPIO37/KSI7	KSI7	I	Internal pull high
63	GPI38/AD0	BAT_ICHG	I	
64	GPI39/AD1	BAT_CONFIG	I	Battery configuration
65	GPIO3A/AD2	BAT_SENSE	I	Battery Voltage Sensor
66	GPIO3B/AD3	BAT_TS	I	Battery Thermal Sensor
68	GPO3C/DA0	DOC	O	Trigger Clock Gen

EC KB3310 Other Pin SETTING

Pin	Pin Name	Signal Name	Type	Note
3	SERIRQ	INT_SERIRQ	I/OD	10K pull high to +3V
4	LFRAME#	LPC_FRAME#	I	
5	LAD3	LPC_AD3	I/O	
7	LAD2	LPC_AD2	I/O	
8	LAD1	LPC_AD1	I/O	
9	VCC	+3VA_EC	P	
10	LAD0	LPC_AD0	I/O	
11	GND	GND	P	
12	PCICLK	CLK_PCI_EC	I	
22	VCC	+3VA_EC	P	
24	GND	GND	P	
33	VCC	+3VA_EC	P	
35	GND	GND	P	
37	ECRST#	EC_RST#	I	100K pull high to +3VA_EC
67	AVCC	+3VACC	P	
69	AGND	AGND	P	
94	GND	GND	P	
96	VCC	+3VA_EC	P	
111	VCC	+3VA_EC	P	
113	GND	GND	P	
119	RD#/SPIDI	SPL_SO	I	
120	WR#/SPIDO	SPL_SI	O	
112	XCLKI	32KXCLKI	I	
123	XCLKO	32KXCLKO	O	
124	V18R	V18R	P	Reserved 1uF to GND
125	VCC	+3VA_EC	P	
128	SPICS#/SELMEM#	SPL_CE#	O	

Pin	Pin Name	Signal Name	Type	Note
70	GPO3D/DA1	LCD_BACKOFF#	O	
71	GPO3E/DA2	CLK_PWRSERVE#	O	
72	GPO3F/DA3	BAT_LL#	O	Battery Low Low
73	GPIO40	AC_OK	I	AC Adaptor Plug in
74	GPIO41	PM_RSMRST#	O	10K pull down to GND
75	GPI42	BAT_IN	I	
76	GPI43	CLRTC_EC	I	
77	GPIO44/SCL1	SMB0_CLK	I/OD	4.7K pull high to +3VA_EC
78	GPIO45/SDA1	SMB0_DAT	I/OD	4.7K pull high to +3VA_EC
79	GPIO46/SCL2	SMB1_CLK	I/OD	10K pull high to +3V
80	GPIO47/SDA2	SMB1_DAT	I/OD	10K pull high to +3V
81	GPIO48/KSO16	KB pin 28	I	for KB type detection
82	GPIO49/KSO17	KB pin 27	I	for KB type detection
83	GPIO4A/PSCLK1	AUO_SCL	O	for AUO, default H at S0
84	GPIO4B/PSDAT1	AUO_SDA	O	for AUO, default L at S0
85	GPIO4C/PSCLK2	AUO_CSB	O	for AUO, default H at S0
86	GPIO4D/PSDAT2	LVDD_EN	I	for AUO 7" Panel
87	GPIO4E/PSCLK3	TP_CLK	I/OD	10K pull high to +3V
88	GPIO4F/PSDAT3	TP_DAT	I/OD	10K pull high to +3V
89	GPIO50/SELIO#	BATSEL_3S	O	Battery series, H:3S, L:4S
90	GPIO52/E51_CS#	CHG_LED_UP#	O	
91	GPIO53/CAPLED	CAP_LED#	O	
92	GPIO54	PWR_LED_UP	O	
93	GPIO55/SCRLED	SCRL_LED#	O	
95	GPIO56	PWR4G_SW#	I	Internal pull high
97	GPX0A00/SDICS#	SPI_MODE#	O	4.7K pull down to GND
98	GPX0A01/SDICLK	SUSC_ON	O	
99	GPX0A02/SDIDO	VSUS_ON	O	
100	GPX0A03	CPU_VRON	O	
101	GPX0A04	SUSB_ON	O	
102	GPX0A05	ICH_PWROK	O	
103	GPX0A06	VOLT_CTRL	O	
104	GPX0A07	CHG_EN#	O	Battery charging enabled
105	GPX0A08	PRECHG	O	
106	GPX0A09	SPI_WP#	O	
107	GPX0A10	OP_SD#	O	Audio OP
108	GPX0A11	BAT_LEARN	O	
109	GPXID0/SDIDI	BATSEL_2P#	O	Battery parallel, H:1P, L:2P~3P
110	GPXID1	NC	O	
112	GPXID2	THRO_CPU	O	Active if CPU temperature over spec
114	GPXID3	SUSB#	I	100K pull down to GND
115	GPXID4	SUSC#	I	100K pull down to GND
116	GPXID5	CPUPWR_GD	I	Pull high to +3V
117	GPXID6	VSUS_GD	I	
118	GPXID7	NC	O	
121	GPIO57	INTERNET#	I	Internal pull high
126	GPIO57/SPICLK	SPI_CLK	O	
127	GPIO59/TEST_CLK	NC	O	

<Core Design>

		Title : EC Pin Define	
ASUSTek Computer INC.		Engineer: Satan He	
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